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     FILE 'INSPEC, HCAPLUS' ENTERED AT 15:05:49 ON 29 APR 2002
L1        522426 S IC OR ICS OR ((INTEGRATED OR LOGIC)(W)(CIRCUIT)) OR ((MICRO)(
L2        470956 S STACK### OR MOUNT? OR PILE OR PILED OR MOUND? OR ATTACH?
L3       2499435 S CONNECT? OR JOIN### OR COMBINE OR CONJOIN? OR CONJUGATE OR CO
L4        676017 S POSTS OR SPHERE OR SPHERES OR BALL OR PLATE  OR BUMP
L5        179230 S DRAIN OR DRIFT OR (ACTIVE OR DIFFUSION OR SOURCE)(2N)(REGION
L6        164687 S GATE OR GATES OR THYRISTOR OR (LOGIC(2N)ELEMENT)
L7             1 S DRAIN CLIP
L8             0 S LEAD()RAIL
L9         28010 S L1 AND L2
L10         1647 S L9 AND L6
L11            6 S L10 AND LEADFRAME
L12            5 DUP REMOVE L11 (1 DUPLICATE REMOVED)
L13          263 S L10 AND L5
L14           67 S L13 AND L3
L15            9 S L14 AND LEAD
L16            9 S L15 NOT (L12 OR L7)
L17           12 S L14 AND L4
L18           10 S L17 NOT (L12 OR L7 OR L16)
L19           10 DUP REMOVE L18 (0 DUPLICATES REMOVED)
L20           48 S L14 NOT (L12 OR L7 OR L16 OR L19)
L21           46 DUP REMOVE L20 Y (2 DUPLICATES REMOVED)
L22          647 S L9 AND L5
L23          263 S L22 AND L6
L24            0 S L23 AND LEADFRAME
L25            6 S L10 AND LEADFRAME
L26          235 S L9 AND LEADFRAME
L27            2 S L26 AND L5
L28            2 S L27 NOT (L12 OR L7 OR L16 OR L19 OR L21)
L29            2 S L26 AND CLIP
L30            2 S L29 NOT (L12 OR L7 OR L16 OR L19 OR L21 OR L28)
L31            0 S L26 AND RAIL
L32            2 S L22 AND CLIP
L33            1 S L10 AND CLIP
L34            2 S (L32 OR L33) NOT (L12 OR L7 OR L16 OR L19 OR L21 OR L28 OR
L35           46 S L21 NOT (L12 OR L7 OR L16 OR L19 OR L28 OR L30 OR L32 OR L
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L12 ANSWER 3 OF 5 INSPEC COPYRIGHT 2002 IEE
AN 1999:6425560 INSPEC DN B2000-01-1350F-025
TI Material property, compatibility, and reliability issues in diamond-enhanced, GaAs-based plastic packages.
AU Fabis, P.M. (St. Gobain Ind. Ceramics, Norton Diamond Film, Northborough, MA, USA)
SO Microelectronics Reliability (Aug. 1999) vol.39, no.8, p.1275-91. 22 refs.
Doc. No.: S0026-2714(99)00040-2
Published by: Elsevier
Price: CCCC 0026-2714/99/$20.00
CODEN: MCRLAS ISSN: 0026-2714
SICI: 0026-2714(199908)39:8L.1275:MPCR;1-P
DT Journal
TC Practical; Theoretical; Experimental
CY United Kingdom
LA English
AB GaAs MESFETs (**chip** and wire/flip-**chip**) and PHEMTs were plastic packaged using CVD diamond (CVDD) in SOIC and QFP, respectively. CVDD compatibility was assessed in terms of thermal, thermo-mechanical and chemical properties, and package spatial arrangement and dimensions. FEA modeling showed optimum thermal/thermo-mechanical designs with: (1) **leadframe**-CVDD substrate overlap configuration; (2) all-metallic assembly process (**die/leadframe attach**); (3) compliant metal GaAs-CVDD interlayer. CVDD surface oxidation gave strong affinity to the polymer encapsulant, resisting >50 cycles of 15 min boiling water immersion and peel tests before failure. Use of these considerations in CVDD-enhanced GaAs plastic packages gave major improvements over Cu **leadframe** packages. GaAs/CVDD plastic package performance milestones were: (a) >50% Theta j reduction for Cu **die**-paddle package (Theta j(**chip**/wire)=127 degrees C and Theta j(flip-**chip**)=141 degrees C for 2.5 W, 1 GHz GaAs MESFET); (b) 96 h, 20 W continuous operation for Theta j(**chip**/wire) of 140 degrees C for a 30 W, 3-6 GHz, GaAs PHEMT; (c) passed MIL STD 883 1000 cycle, -55 to 125 degrees C exposure; (d) passed HAST (110 degrees C, 200 h, 85% RH, 3.1 atm). S-parameter electrical tests of metallized CVDD coplanar transmission lines and diamond-enhanced coplanar GaAs flip-**chip** MESFET packages showed: (a) transmission line performance equivalent to Al2O3 (<1.5 dB at 20 GHz, VSWR=1.2:1) and (b)

near identical performance of unpackaged devices and diamond-enhanced plastic encapsulated packages. The results show that diamond can be processed/packaged using conventional techniques and provide superior performance and high reliability.

L12 ANSWER 4 OF 5 INSPEC COPYRIGHT 2002 IEE
AN 1997:5767069 INSPEC DN B9801-1210-020
TI Power cycling reliability of IGBT power modules.
AU Sankaran, V.A.; Chen, C.; Avant, C.S.; Xu, X. (Sci. Res. Lab., Ford Motor Co., Dearborn, MI, USA)
SO IAS '97. Conference Record of the 1997 IEEE Industry Applications Conference Thirty-Second IAS Annual Meeting (Cat. No.97CH36096) New York, NY, USA: IEEE, 1997. p.1222-7 vol.2 of 3 vol. xxxiv+2394 pp. 4 refs.
Conference: New Orleans, LA, USA, 5-9 Oct 1997
Price: CCCC 0 7803 4067 1/97/$10.00
ISBN: 0-7803-4067-1
DT Conference Article
TC Experimental
CY United States
LA English
AB The goal of this study was to understand the power cycling reliability of IGBT power modules. These power modules are made up of multi-layer **stacks** and consist of multiple power **dice** in parallel. The interconnection schemes within the module include **leadframes** soldered to substrate, **die attachment** using solder and wirebonds. Thermal and power cycling fatigues material interfaces because of the CTE mismatch between dissimilar materials. In addition, wirebonds on the **dice** are prone to debonding because of the thermally induced stresses. Tests were designed to understand the power cycling reliability of these large transistor modules. Results from the tests are summarized in this paper.

L12 ANSWER 5 OF 5 INSPEC COPYRIGHT 2002 IEE
AN 1983:2109391 INSPEC DN B83049285
TI Plastic encapsulated GaAs MESFET.
AU Wetzel, C.; Frary, J. (Motorola Inc., Schaumburg, IL, USA)
SO Motorola Technical Developments (March 1983) vol.3, p.72. 0 refs.
CODEN: MTDEDP ISSN: 0887-5286
DT Journal
TC Practical
CY United States
LA English
AB Describes a gallium arsenide depletion-mode low-noise MESFET which is passivated with a Dupont polyimide and encapsulated in a plastic package. The process employs Dupont P12545 polyimide as the passivation layer, epoxy **die attach** to a Macro-X **leadframe**, and encapsulation with Hysol 130 resin. Studies have shown that neither the polyimide nor the plastic packaging degrades the device RF performance, while silicon nitride does. This process also offers the advantages of lower cost and easier fabrication.

L7 ANSWER 1 OF 1 INSPEC COPYRIGHT 2002 IEE
AN 2002:7206840 INSPEC DN B2002-04-2560R-076
TI Dual thermal paths double power handling for surface-mount MOSFETs.
AU Morrison, D.G.
SO Electronic Design (21 Jan. 2002) vol.50, no.2, p.33-6
Published by: Penton Media
Price: CCCC 0013-4872/02/$2.00+1.00
CODEN: ELODAW ISSN: 0013-4872
SICI: 0013-4872(20020121)50:2L.33:DTPD;1-D
DT Journal
TC Practical; Experimental
CY United States
LA English
AB International Rectifier's DirectFET is a surface-mount package that improves MOSFET performance by lowering both the package's electrical and thermal resistance. It does so with a design that permits direct attachment of the die to the customer's PC board via solderable pads on the chip and through attachment to a copper **drain clip** that allows double-sided cooling. The latter feature is an industry first for a surface-mount power package.

L16 ANSWER 1 OF 9 INSPEC COPYRIGHT 2002 IEE
AN 2000:6754280 INSPEC DN B2000-12-2570D-043
TI RTP for advanced device fabrication using shallow, elevated, and silicided junctions.
AU Osburn, C.M. (Center for Adv. Electron. Mater. Process., North Carolina State Univ., Raleigh, NC, USA)
SO Advances in Rapid Thermal Processing. Proceedings of the Symposium. (Electrochemical Society Proceeding Vol.99-10)
Editor(s): Roozeboom, F.; Gelpey, J.C.; Ozturk, M.; Nakos, J.
Pennington, NJ, USA: Electrochem. Soc, 1999. p.197-206 of xii+452 pp. 17 refs.
Conference: Seattle, WA, USA, 3-6 May 1999
Sponsor(s): Electrochem. Soc
ISBN: 1-56677-232-X
DT Conference Article
TC Practical; Experimental
CY United States
LA English
AB Rapid thermal processing is needed to minimize motion of dopants in CMOS device channels and in extension junctions. The thermal cycle associated with growth or deposition of the **gate** dielectric is shown to affect the final channel doping profile, and a variety of deposited **gate stack** dielectrics have been used successfully to minimize the thermal budget. The use of silicides as diffusion sources (SADS) reduces transient enhanced dopant diffusion and junction leakage; more importantly, it maximizes the doping concentration at the metal (silicide)-semiconductor contact and thereby minimizes the interfacial contact resistivity. However, junctions beneath the silicide must have sufficiently low sheet resistance, i.e. they must be sufficiently deep in order to minimize the overall contact resistance. This consideration requires that the SADS junction anneal be around 10 s at 950 degrees C or a 1050 degrees C spike anneal, thus the silicide technology must be thermally stable under these conditions. To be useful, elevated source/**drain** processes must employ RTP in order to minimize the impact on the extension junction depth. Epi faceting is an issue for ESD devices. On one hand, faceting is needed to confine the epi along the edges of trench isolation; on the other hand, facets can **lead** to locally deeper junctions and silicides. When facets are present, special care must be taken to avoid junction penetration by the silicide. Using SADS technology in ESD devices is a good way to **combine** the advantages of each, and good device characteristics have been observed.

L16 ANSWER 2 OF 9 INSPEC COPYRIGHT 2002 IEE
AN 1997:5652230 INSPEC DN B9709-2860-017
TI La0.5Sr0.5CoO3/Pb(Nb0.04Zr0.28Ti0.68)O3 /La0.5Sr0.5CoO3 thin film heterostructures on Si using TiN/Pt conducting barrier [capacitors].
AU Yang, B.; Aggarwal, S.; Dhote, A.M.; Song, T.K.; Ramesh, R. (Dept. of Mater. & Nucl. Eng., Maryland Univ., College Park, MD, USA); Lee, J.S.
SO Applied Physics Letters (21 July 1997) vol.71, no.3, p.356-8. 12 refs.
Doc. No.: S0003-6951(97)01229-1
Published by: AIP
Price: CCCC 0003-6951/97/71(3)/356/3/$10.00
CODEN: APPLAB ISSN: 0003-6951
SICI: 0003-6951(19970721)71:3L.356:5502;1-X
DT Journal
TC Practical; Experimental
CY United States
LA English

AB A high density ferroelectric memory process flow requires the integration of conducting barrier layers to **connect** the **drain** of the pass-**gate** transistor to the bottom electrode of the ferroelectric **stack**. We are studying the effect of crystallinity of the TiN/Pt barrier layer with Si **wafers** on the ferroelectric properties of La0.5Sr0.5CoO3/Pb(Nb0.04Zr0.28Ti0.68)O3 /La0.5Sr0.5CoO3 (LSCO/PNZT/LSCO) capacitors. Structural studies indicate complete phase purity (i.e., fully perovskite) in both epitaxial and polycrystalline materials. The polycrystalline capacitors show lower remnant polarization and coercive voltages. However, the retention, fatigue, and imprint characteristics are similar, indicating minimal influence of crystalline quality on the ferroelectric properties.

L16 ANSWER 3 OF 9 INSPEC COPYRIGHT 2002 IEE
AN 1985:2426339 INSPEC DN B85023774
TI Complementary MOSFETs make switched and linear power control easier.
AU Ruble, R.; Alexander, M. (Siliconix Inc., Santa Clara, CA, USA)
SO Electronic Design (29 Nov. 1984) vol.32, no.24, p.245-54. 0 refs.
CODEN: ELODAW ISSN: 0013-4872
DT Journal
TC Practical; Product Review
CY United States
LA English
AB Double-diffused power MOSFETs can handle a lot of power in linear and switching applications, some of which demand the use of paired p- and n-channel DMOS devices, but finding the right complementary pair is not easy, especially if the two must be matched for both dynamic and static characteristics. Moreover, to ensure that they stay matched as temperature varies, two power packages must then be **mounted** on one heat sink. The members of the MPP500 family of power MOSFETs each contain two DMOS FET **dice** one p-channel and the other n-channel. Instead of needing separate packages, the **dice** are seated side by side in one TO-220 package with five **leads**, and they share the same heat sink. The result looks just like a CMOS logic inverter with the usual common **drain connection**-except that it can dissipate 20 W. Also, since the two **dice** are the same size, their input capacitances are virtually identical, and the resulting symmetry of their waveforms when they switch on or off simplifies the design of **gate** -driving circuits in switching applications.

L16 ANSWER 4 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:934641 HCAPLUS
TI High current capacity semiconductor device package and **lead** frame with large area **connection** posts and modified outline
IN Woodworth, Arthur; Ewer, Peter R.; Teasdale, Ken
PA UK
SO U.S. Pat. Appl. Publ.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001054752	A1	20011227	US 1998-103035	19980623
PRAI	US 1998-84224P	P	19980505		

AB A **lead** frame for a high power semiconductor device **die** has three external **lead** conductors, the outer two of which are reentrantly bent outwardly from the center of the **lead** frame. When the **lead** frame is overmolded, the outer conductors are

spaced from a central conductor by an increased creepage distance along the plastic surface of the housing. Further, the **lead** sequence of the exterior **leads** is **gate**, source, **drain** for a power MOSFET. The post area for wire bonding to the source post is enlarged to permit wire bonding with at least three bond wires. The external conductors can be downwardly bent to form a surface **mount** device. The cross-sectional area of the external conductors is substantially enlarged, although only a small enlargement of the circuit board hole is needed. The package outline has a long flat area centered over the main **die** area, with a tapered end surface which allows the package to pry open a **mounting** spring for surface **mounting** of the package.

L16 ANSWER 5 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:848581 HCAPLUS
TI Power semiconductor package and method for making the same
IN Kuo, Frank
PA Taiwan
SO U.S. Pat. Appl. Publ.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001044167	A1	20011122	US 2001-879367	20010612
PRAI	TW 2000-89109555	A	20000518		

AB A power semiconductor **die** has a **drain** contact, a source contact, and a **gate** contact. A **lead** frame has first, second, and third terminals. A metal sheet has first and second contacting portions and a bridging portion interconnecting the first and second contacting portions. The power semiconductor **die** is **mounted** on the **lead** frame such that the **drain** contact is **connected** to the first terminal. The metal sheet is **attached** to the top surface of the power semiconductor **die** and the second and third terminals of the **lead** frame such that the source contact and the second terminal are **connected** to the first contacting portion, and such that the **gate** contact and the third terminal are **connected** to the second contacting portion. The bridging portion is subsequently cut for disconnecting electrically the first and second contacting portions.

L16 ANSWER 6 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:478307 HCAPLUS
DN 127:213438
TI La0.5Sr0.5CoO3/Pb(Nb0.04Zr0.28Ti0.68)O3/La0.5Sr0.5CoO3 thin film heterostructures on Si using TiN/Pt conducting barrier
AU Yang, B.; Aggarwal, S.; Dhote, A. M.; Song, T. K.; Ramesh, R.; Lee, J. S.
CS Department of Materials and Nuclear Engineering and Center for Superconductivity Research, University of Maryland, College Park, MD, 20742, USA
SO Appl. Phys. Lett. (1997), 71(3), 356-358
CODEN: APPLAB; ISSN: 0003-6951
PB American Institute of Physics
DT Journal
LA English
AB A high d. ferroelec. memory process flow requires the integration of conducting barrier layers to **connect** the **drain** of the pass-**gate** transistor to the bottom electrode of the ferroelec.

stack. We are studying the effect of crystallinity of the TiN/Pt barrier layer with Si **wafers** on the ferroelec. properties of La0.5Sr0.5CoO3/Pb(Nb0.04Zr0.28Ti0.68)O3/La0.5Sr0.5CoO3 (LSCO/PNZT/LSCO) capacitors. Structural studies indicate complete phase purity (i.e., fully perovskite) in both epitaxial and polycryst. materials. The polycryst. capacitors show lower remnant polarization and coercive voltages. However, the retention, fatigue, and imprint characteristics are similar, indicating minimal influence of cryst. quality on the ferroelec. properties.

L16 ANSWER 7 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:313476 HCAPLUS
DN 120:313476
TI GaAs Schottky-barrier FETs
IN Ose, Yasushi
PA Yamagata Nippon Denki Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 05267349	A2	19931015	JP 1992-58674	19920317
JP 2919159	B2	19990712		

AB In a GaAs Schottky-barrier FET, which has a **gate** electrode and **drain**/source electrodes in, resp., rectifying and resistive contact with the active reion of a GaAs substrate, a **drain** electrode **lead** pattern, which is **connected** with a transistor-**chip-mounting** container through a bonding wire, and formed outside of the **active region**, is divided into a no. of parts, which are elec. **connected** through the pattern of a metal film (e.g., AuGe/Ni) which has same quality and thickness as the metal film, which the **drain**/source electrodes are in resistive contact with. The FET has stable high frequency characteristic.

L16 ANSWER 8 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1970:471268 HCAPLUS
DN 73:71268
TI **Integrated circuits** with complementary elements
IN Legat, Wilhelm H.; Dixon, Alan F.
PA Raytheon Co.
SO U.S., 5 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 3514845	A	19700602	US 1968-753119	19680816

AB An **integrated-circuit** device is described which includes a no. of complementary MOSFETs (metal-oxide-semiconductor field-effect transistors). Each transistor includes spaced **source** and **drain regions** of similar type which are located within a common region of opposite type. Overlying the space between the regions is a metal **gate** electrode which is insulated from the surface of the device by a layer of SiO2. E.g., 2 transistors each comprise n-type **source** and **drain regions**,

these regions being disposed within resp. p-regions located in the n-type **wafer** which forms the matrix. Between the 2 transistors is a 3rd transistor which comprises spaced p-type **source** and **drain regions** directly located in the n-type matrix. The surface is coated with a layer of SiO2 with suitably shaped apertures which exposes surfaces of the **source** and **drain regions** of the transistors. Elec. contacts are made through the apertures by layers of Au, Ni, Al, etc. deposited in the apertures and which are each provided with portions overlying adjacent portions of the insulating layer to provide relatively large or broad contact areas to which **leads** can be easily **attached**. Above the **area** between **source** and **drain regions** is the **gate** electrode, which is spaced from the surface by portions of the oxide layer. With respect to a single n-type FET, by applying a pos. potential to the **gate** equal to or greater than the crit. magnitude, an n-type inversion layer or channel is produced, **connecting** the n-diffused **source** and **drain regions** for imparting a source-to-**drain** conductance. In the complementary p-type device, a neg. potential is applied to the **gate** to form a p-type inversion layer or channel. The transistor region between the inversion layer and substrate functions like a p-n junction and remains reverse biased at all times. When the potential applied to a **gate** is below the crit. value, the impedance between the source and **drain** is very high and corresponds to a reverse-biased planar Si diode. The FETs in the circuit device are perfectly complementary, since all elements are capable of being precisely duplicated in size, shape, and spatial relation.

L16 ANSWER 9 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1967:41737 HCAPLUS
DN 66:41737
TI Tellurium thin-film field-effect devices
IN Weimer, Paul K.
PA Radio Corp. of America
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 3290569		19661206	US	19640214

AB Te thin-film, field-effect, solid-state devices are described which can be prepd. entirely by deposition of thin films on an insulating substrate; by using an elemental semiconductor having high charge-carrier mobility; and by fabricating these devices without heating the substrate. E.g., the device consists of an insulating substrate, i.e., a plate of glass, ceramic, or fused quartz, or the substrate can be a synthetic resin or plastic. On one face of the substrate, 2 spaced electrodes are deposited. These can be metals (In, Cu, Au, etc.) and can be deposited on thin films by masking and evapg. techniques. The gap between the electrodes is .apprx.0.1-20 .mu.. A 50-5000-A. layer of cryst. Te is deposited on the substrate to cover part of the 2 electrodes and the gap. An insulating film (e.g., SiO, SiO2, CaF2, Al2O3, or ZnS) is deposited on part of the semiconductor layer. A **gate** or control electrode is deposited on the insulating film opposite the gap. The control electrode can be an alloy or metal, e.g., Au, or Al, and can be deposited on the insulating film by masking and evapg. techniques. Elec. **lead** wires are **attached** to those parts of the spaced electrodes not covered by

the Te layer and to the control electrode by a metallic paste. An advantage of the device is that the Te layer can be deposited on the substrate without heating it. As a result, insulating substrates having low m.ps. can be used. In addn., a rectifying barrier, e.g., a p-n junction, is not required in the Te layer. The device operates by field-effect control of majority charge carriers. The source and **drain** electrodes are both ohmic **connections** to the Te layer. The control electrode forms an insulated **coupling** through the insulating film to the Te layer. The insulated **coupling** is blocking in both directions. The semiconductive layer can be made very **uniform** in compn. and properties and may be polycryst. As a result of its high mobility and narrow energy gap, Te is .gtoreq.3 orders of magnitude more conductive than other materials used (CdS and CdSe). The p-type thin-film transistor is superior to others and can be combined on a single substrate with n-type transistors to form **integrated circuits** whose characteristics are superior to circuits having transistors of only 1 type or circuits of 2 types made with prior p-type devices.

L19 ANSWER 1 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:28277 HCAPLUS
TI Resin seal type semiconductor device. [Machine Translation].
IN Suzuki, Takeshi; Yoneda, Tatsuo
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2002009219	A2	20020111	JP 2000-188191	20000622

AB [Machine Translation of Descriptors]. As increase of the impedance in the high lap wave motion work in power MOSFET and the like is held down, the small-sized surface **mounted** type semiconductor device which assures the decrease of noise is offered. The **drain** electrode terminal 31 which corresponds with each electrode of the semiconductor **chip** which is installed in the frame baseplate 13 which loads semiconductor **chip** 12 and this frame baseplate, source electrodes terminal 33, **gate** electrode terminal the separation doing the source electrodes of 35 and the tip/**chip**, provides the GND electrode terminal 37 which tie with the GND electrode which formed between the **gate** electrode terminal and the source electrodes terminal, gold wire 32 of low impedance and 34 or **connects** each electrode of the source, the **gate** and the GND and between the electrode terminals with the metallic **plate**. In addition in order for back of the frame baseplate to touch to the appearance of the printed circuit board directly, resin seal is done.

L19 ANSWER 2 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:593211 HCAPLUS
TI Vertical conduction flip-**chip** device with **bump** contacts on single surface
IN Kinzer, Daniel M.; Arzumanyan, Aram; Sammon, Tim
PA International Rectifier Corporation, USA
SO PCT Int. Appl.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
WO 2001059842	A1	20010816	WO 2001-US4164	20010209

PI W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM
RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG

PRAI US 2000-181504P P 20000210
US 2000-224062P P 20000809

AB A flip-**chip** MOSFET structure has a vertical conduction semiconductor **die** (30) in which the lower layer of the **die** is **connected** to a **drain** electrode (32) on

the top of the **die** by a diffusion sinker or conductive electrode. The source (31) and **gate** (33, 34) electrodes are also formed on the upper surface of the **die** and have coplanar solder **balls** (40, 41, 43) for **connection** to a circuit board. The structure has a **chip** scale package size. The back surface of the **die**, which is inverted when the **die** is **mounted** may be roughened or may be metallized to improve removal of heat from the **die**. Several separate MOSFETs can be integrated side-by-side into the **die** to form a series **connection** of MOSFETs with respective source and **gate** electrodes at the top surface having solder **ball connectors**. Plural solder **ball connectors** may be provided for the top electrodes and are laid out in respective parallel rows. The **die** may have the shape of an elongated rectangle with the solder **balls** laid out symmetrically to a diagonal to the rectangle.

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L19 ANSWER 3 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:906047 HCAPLUS
TI High frequency semiconductor device
IN Maeda, Masahiro; Nakamura, Morio; Yoshida, Takayuki; Yamazaki, Masazumi
PA Matsushita Electric Industrial Co., Ltd., Japan
SO U.S., 34 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6166436	A	20001226	US 1998-60600	19980415
	JP 11003916	A2	19990106	JP 1998-106799	19980416
PRAI	JP 1997-99430	A	19970416		

AB A high frequency semiconductor device includes a substrate having a substantially flat principal surface, with a predetermined circuit pattern including at least an input line, an output line, and a ground electrode provided on the principal surface; and a transistor which has a **drain** electrode, a source electrode, and a **gate** electrode and is **mounted** on the substrate by a flip **chip mounting**. The source electrode and the ground electrode are **connected** to each other by a first **bump** in the flip **chip mounting**.

RE.CNT 16 THERE ARE 16 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L19 ANSWER 4 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:864562 HCAPLUS
TI Optical bond type semiconductor relay. [Machine Translation].
IN Kishida, Takashi; Suzumura, Masahiko; Suzuki, Yuji; Hayasaki, Yoshiki; Shirai, Yoshifumi; [NAME NOT TRANSLATED], Masamichi; Yoshida, Takeshi
PA Matsushita Electric Works, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000340830	A2	20001208	JP 1999-147326	19990526

AB [Machine Translation of Descriptors]. The insertion loss for the high frequency signal is decreased, the optical bond type semiconductor relay which can be stabilized is offered. In the printed wiring baseplate 36 where the integration horizontal MOSFET tip/**chip** 21 which 1 opposite or more was accumulated the semiconductor component as the horizontal structural component where each electrode of the **drain**, the **gate** and the source is formed to one surface side of the identical baseplate and light absorbent tip/**chip** 6 and luminous component 1 is **mounted** and aforementioned printed wiring baseplate 36 being provided in the signal transmission line which the formation is done, the aforementioned tip/**chip** having with the **bump** which the bonding is done, it becomes. Therefore, making wiring inside the tip/**chip** where the semiconductor component above pair the wiring difference is short, furthermore that tip/**chip** by directly bumping **connects** on printed wiring baseplate 36, the decrease the inductance component it is possible, to be able to point, it is possible to decrease the insertion loss for the high frequency signal.

L19 ANSWER 5 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:118081 HCAPLUS
DN 136:143546
TI Silicon-on-insulator device of reversed **stacked** capacitor structure and manufacturing method thereof
IN Jung, Moung Jun
PA Hyundai Electronics Ind. Co., Ltd., S. Korea
SO Repub. Korean Kongkae Taeho Kongbo, No pp. given
CODEN: KRXXA7
DT Patent
LA Korean
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	KR 2000027628	A	20000515	KR 1998-45583	19981028

AB A silicon-on-insulator (SOI) device having reversed **stacked** capacitor structure and manufg. method the same to prevent from reducing device characteristics resulted in the parasitic bipolar junction transistor (BJT) effect or kink effect causing floating body in SOI device having RSC cell structure. A field oxide film is formed on both a cell area of a semiconductor substrate and peripheral circuit area. A transistor including a **gate** oxide film, a **gate** electrode, a lightly-doped **drain** (LDD), an LDD spacer film and a source/**drain** is formed. And a storing electrode contact hole is formed by depositing and removing a 1st dielec. film, then, a capacitor including a capacitor storing electrode, an elec. film, a capacitor upper electrode. A 2nd dielec. film is deposited over an entire surface of the capacitor and a supporting **plate** is conjugated to an upper part of the 2nd dielec. film. And a 3rd dielec. film is formed after etching the field oxide film to be being remained a const. thickness of the upper part of the field oxide film by reversing an **wafer**. A bit line contact hole is formed by etching the 3rd dielec. film placed in the source/**drain**. A plug ion injection area **connected** elec. to the source/**drain** is formed by performing the ion injection with impurities type such as the source/**drain**, and, a bit line is formed to be filled into the contact hole.

L19 ANSWER 6 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:192270 HCAPLUS
DN 128:277949
TI **Integrated circuit** and its manufacture
IN Sasashima, Katsuhiro
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 13 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 10079480	A2	19980324	JP 1996-235342	19960905

AB The process comprises formation of a no. of wiring layers with a no. of insulating layers between them on a semiconductor substrate after formation of semiconductor devices; etching the insulating layers to form 1st contact holes reaching the semiconductor devices and filling the holes with plugs; deposition of an insulating film on the wiring layer and the plugs and etching the insulating film, simultaneously forming 2nd and 3rd contact holes reaching the wiring layer and the plugs, resp., in prepn. of a multilayer wiring **integrated circuit**; formation of a 1st insulating film on MISFETs for selection of memory cells and those on peripheral circuits; etching the 1st insulating film, forming contact holes reaching the **source** and **drain regions** of the MISFETs for selection of the memory cells and filling the holes with 1st plugs; forming bit lines on the 1st insulating film, forming a 2nd insulating film on them, and etching, forming contact holes reaching the plugs above the **source** or **drain regions** of the MISFETs and filling the holes with 2nd plugs; formation of capacitors for information storage; etching the 2nd and 1st insulating films, forming contact holes reaching the **source** and **drain regions** or the **gate** electrodes, and filling the holes with 3rd plugs. A 3rd insulating film is formed on the capacitors and etched, simultaneously forming contact holes reaching the **plate** electrodes of the capacitors and the 3rd plugs on the peripheral circuits; a conductor film formed on the 3rd insulating film is patterned, simultaneously forming wirings **connected** to the **plate** electrodes of the capacitors and those **connected** to the **source** or **drain regions** or the **gate** electrodes of the MISFETs on the peripheral circuits through the 3rd plugs, for prepn. of an **integrated circuit** contg. DRAMs which have memory cells with **stacked** capacitor structures. The bit lines and the 2nd and 3rd plugs may be made of: polycryst. Si and a refractory metal or its silicide; polycryst. Si or a metal; and a metal, resp. Excess etching of the bottoms of contact holes of a small aspect ratio, which **connect** an upper wiring to a lower wiring, is prevented in simultaneous formation of the contact holes with those of a large aspect ratio, which **connect** the wiring to the devices, by preliminary filling of the contact holes of the large aspect ratio with plugs.

L19 ANSWER 7 OF 10 INSPEC COPYRIGHT 2002 IEE
AN 1989:3353012 INSPEC DN B89029734
TI Silicon MOS caps carry GaAs MMICs to singular bias.
AU Sabo, D.; Ou, W.; Hundley, B. (Varian Associates Inc., Santa Clara, CA, USA); Nuttall, J.; Nelson, S.
SO Microwaves & RF (Dec. 1988) vol.27, no.13, p.103-8. 1 refs.
CODEN: MIRFDL ISSN: 0745-2993

DT Journal
TC Practical
CY United States
LA English
AB Designers of GaAs monolithic microwave **integrated circuits** (MMICs) often **connect** the source terminal of field-effect transistors (FETs) directly to the ground plane. Although such configurations maximize high-frequency performance, they also require dual-polarity sequential biasing of **gate** and **drain** terminals. However, MMICs with grounded-source FETs can be **mounted** on a parallel-**plate** capacitor, enabling operation from a single voltage supply. A silicon metal-oxide-semiconductor (MOS) capacitor can be used to float the FET source terminals from ground at DC. **Attached** to a carrier using epoxy, the capacitor provides grounding at RF while isolating source terminals at DC. Self-bias is achieved by grounding **gate**-bias terminals and **connecting** a resistor between source terminals and ground.

=> D BIB AB 1-2

L28 ANSWER 1 OF 2 INSPEC COPYRIGHT 2002 IEE
AN 1996:5364625 INSPEC DN B9610-4260D-018
TI High-efficiency ZnCdSe-ZnSSe-ZnMgSSe green and blue light-emitting diodes.
AU Nakayama, N.; Itoh, S.; Ishibashi, A. (Res. Center, Sony Corp., Yokohama, Japan); Mori, Y.
SO Proceedings of the SPIE - The International Society for Optical Engineering (1996) vol.2693, p.36-42. 14 refs.
Published by: SPIE-Int. Soc. Opt. Eng
Price: CCCC 0 8194 2067 0/96/$6.00
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1996)2693L.36:HEZZ;1-1
Conference: Physics and Simulation of Optoelectronic Devices IV. San Jose, CA, USA, 29 Jan-2 Feb 1996
Sponsor(s): SPIE
DT Conference Article; Journal
TC Practical; Experimental
CY United States
LA English
AB Molecular beam epitaxy (MBE) has been used to grow II-VI green and blue light-emitting diodes (LEDs) on n-GaAs substrates. The main structure consists of a ZnCdSe-ZnSSe triple quantum-well **active region**, ZnSSe carrier confining layers, ZnMgSSe cladding layers, and a p-ZnTe/p-ZnSe multiple quantum-well contact region. The LED **chips**, 0.3*0.3 mm2 in size, were **mounted** on LED **leadframes** and were encapsulated in epoxy. The devices produce light output powers of 3.5 mW (513 nm) and 1.5 mW (486 nm) for a direct current (DC) of 20 mA at room temperature. The corresponding external quantum efficiencies are 7.2% for the green, and 2.9% for the blue LEDs. In particular, the blue LED operated at a low applied voltage of 2.63 V for 20 mA. An aging test showed a half-intensity lifetime of 1000 hours for the candela-class blue LED under a constant DC drive current of 10 mA at an ambient temperature of 27 degrees C.

L28 ANSWER 2 OF 2 INSPEC COPYRIGHT 2002 IEE
AN 1995:4874613 INSPEC DN B9503-2570-025
TI Memory package with LOC structure using new adhesive material.
AU Nakayoshi, H.; Izawa, N. (Semicond. Adv. Packaging Eng. Dept., Toshiba Corp., Kawasaki, Japan); Ishikawa, T.; Suzuki, T.
SO 1994 Proceedings. 44th Electronic Components and Technology Conference (Cat. No.94CH3241-7)
New York, NY, USA: IEEE, 1994. p.575-9 of xvii+1118 pp. 0 refs.
Conference: Washington, DC, USA, 1-4 May 1994
Sponsor(s): IEEE Components Hybrids & Manuf. Technol. Soc.; Electron. Ind. Assoc
Price: CCCC 0569-5503/94/0000-0575$3.00
ISBN: 0-7803-0914-6
DT Conference Article
TC Practical
CY United States
LA English
AB The LOC (Lead On **Chip**) structure has been considered as an effective technology to encapsulate a large LSI memory **chip** into a small package. The main feature of the structure is contact of **leadframes** onto the **active chip area** with adhesive sandwiched in between. Therefore, the design concept of LOC greatly depends on the characteristics of the adhesive layer. The key

technologies for LOC development are summarized as: 1. To lessen damage on **chip** during **die-attach** and wire bonding; 2. To secure sufficient wire bendability above the organic adhesive; and 3. To reduce package crack rate during the solder reflowing process. We have developed a new adhesive tape which is composed of single-layer thermoplastic polyimide siloxanes. Due to the absence of a base film, the single layer adhesive can be fabricated to any desirable thickness. During its softening process, the thick adhesive film encloses dust that, otherwise, could damage the **chip** surface. These properties, by providing a large Young's modulus of the film at high temperature and contamination-free lead surface, enable us to secure sufficient lead-wire bendability. The other materialistic advantage of the adhesive is its low moisture absorption. The low moisture absorption results in high resistance against package crack caused by the solder reflowing process. In this paper, we describe how we have selected the LOC adhesive tape through the evaluations of the assembly process and have successfully developed a highly productive and reliable memory package with LOC structure.

L30 ANSWER 1 OF 2 INSPEC COPYRIGHT 2002 IEE
AN 2001:6933863 INSPEC DN B2001-07-2240-001
TI The back-end process. III. **Die attach**.
AU Mueller, B. (Alphasem AG, Berg, Switzerland)
SO Advanced Packaging (March 2001) vol.10, no.3, p.47-51. 0 refs.
Published by: PennWell Publishing
CODEN: ADPAFZ ISSN: 1065-0555
SICI: 1065-0555(200103)10:3L.47:BPA;1-V
DT Journal
TC General Review; Practical
CY United States
LA English
AB In the past, most **IC** packages used wirebonding as the interconnect technology between **chip** and **leadframe**. Typically, several heavy wirebonds were used for power applications to give an appropriate connection for the higher currents. These heavy wirebonds have been increasingly replaced by **clip** (bridge) technology, whereby all of the heavy wires are replaced by one **clip** that connects the **leadframe** to the source of the **chip**. With the introduction of new interconnect technologies, companies have begun to produce devices on metal **leadframes** with flip **chip** interconnect technology instead of wirebond connections. In an SO-6 package using flip **chip** connections for all I/Os, each I/O has a solder ball and is directly bonded on to the appropriate **leadframe**. The micro **leadframe** package (MLP) (also called leadless plastic **chip** carrier (LPCC), quad flatpack no-leads (QFN), micro **leadframe** (MLF), etc.) design uses solder balls for all of the lead connections and heat dissipation requirements; additionally, the solder balls maintain the electrical properties of the ground plate through the middle metal pad. There are numerous other potential flip **chip** packaging solutions on metal **leadframes**. Other designs being considered are combinations of flip **chip** interconnect with **clip**/bridge **attach** technology to further improve the electrical and thermal properties of performance-driven applications. **Clip**/bridge **attach** technology was introduced a number of years ago and replaces several heavy wirebonds with a simple metal **clip**.

L30 ANSWER 2 OF 2 INSPEC COPYRIGHT 2002 IEE
AN 1989:3362547 INSPEC DN B89029905
TI Sockets: considerations as an alternative to direct surface **mounting** of components.
AU Pellerite, P.; Suhl, D. (Digital Equipment, Marlboro, MA, USA)
SO Fourth IEEE/CHMT European International Electronic Manufacturing Technology Symposium. Proceedings 1988 (IEEE Cat. No. 88CH2629-4) New York, NY, USA: IEEE, 1988. p.89-91 of 133 pp. 3 refs.
Conference: Neuilly sur Seine, France, 13-15 June 1988
Sponsor(s): IEEE
Price: CCCC CH2629-4/88/0000-0089$01.00
DT Conference Article
TC Experimental
CY United States
LA English
AB Because the surface **mounting** process results in plastic package cracking, it has been suggested that sockets be used to avoid the problem. The authors examine the reliability of plastic leaded **chip** carriers (PLCCs) in two commonly used sockets. Components are found to have different planarity problems than are commonly found in surface-

mount assembly. The engineering factors considered in choosing the appropriate **leadframe** material must change when sockets are used. There are also serious vibration-induced problems which limit the number of manufacturing application areas in which sockets may be of reliable use. Restraining **clips** placed over the devices were examined to determine if simple modifications could be implemented to improve the vibration-induced problems. Dissimilar coatings between the package leads and the socket contacts are examined and discussed, as is the environmental stress range over which these sockets are of practical use in a manufacturing environment.

L34 ANSWER 1 OF 2 INSPEC COPYRIGHT 2002 IEE
AN 1988:3023071 INSPEC DN B88000174
TI A plastic power package without supplementary insulation.
AU Howarth, N.
SO Elettronica Oggi (Sept. 1987) no.46, p.61-2, 65. 0 refs.
CODEN: ELOGDA ISSN: 0391-6391
DT Journal
TC Practical; Product Review
CY Italy
LA Italian
AB The widely used TO-220 package (a plastic container with metallic base) for transistors, **thyristors** and voltage regulators, is frequently subject to trouble due to overheating of the **chip** due to badly applied or inadequate insulation. The author describes a new package, the SOT-186, which overcomes this difficulty by being **mountable** without additional insulation, requiring only a simple spring **clip** as screw to bring it into direct contact with the heat sink. The construction of the package is described and its electrical and thermal characteristics tabulated.

L34 ANSWER 2 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:748161 HCAPLUS
DN 135:281708
TI Design and fabrication of a **chip** scale surface **mounted** MOSFET device
IN Standing, Martin; Schofield, Hazel Deborah
PA International Rectifier Corporation, USA
SO PCT Int. Appl., 23 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2001075961	A1	20011011	WO 2001-US10074	20010329
	W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, YU, ZA, ZW				
	RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG				
	US 2001048116	A1	20011206	US 2001-819774	20010328
PRAI	US 2001-194522P	P	20000404		
	US 2001-819774	A	20010328		
	US 2000-194522P	P	20000404		

AB A **chip** scale package has a MOSFET **die** which has a top electrode surface covered with a layer of a photosensitive liq. epoxy photolithog. patterned to expose portions of the electrode, and to act as a passivation layer or solder mask. A solderable contact layer is formed over the remaining portions of the layer of liq. epoxy. Each individual **die** is **mounted drain** side down in a metal **clip** or is **mounted drain** side down in a can with a **drain** electrode disposed coplanar with a flange extending from the can bottom.

L35 ANSWER 1 OF 46 INSPEC COPYRIGHT 2002 IEE
AN 2000:6558047 INSPEC DN B2000-05-1350H-033
TI An efficient on-**wafer** production test system for MMW power MMICs with diagnostic flag capability.
AU Freitag, R.G.; Renaldo, K.M.; Burns, J.G.; Henry, H.G. (Electron. Sensors & Syst. Sector, Northrop Grumman Corp., Baltimore, MD, USA)
SO 1999 GaAs MANTECH Conference. Digest of Papers
St. Louis, MO, USA: GaAs MANTECH, 1999. p.103-6 of 256 pp. 2 refs.
Conference: Vancouver, BC, Canada, 19-22 April 1999
Sponsor(s): Siemens; Sanders; American Xtal Technology; Raytheon Microelectronics; Fujitsu Compound Semiconductor Inc.; Kopin Corp.; Emcore Corp; GaAsTEK
ISBN: 1-893580-00-8
DT Conference Article
TC Practical; Experimental
CY United States
LA English
AB An on-**wafer** production test system has been developed which provides 100% DC and RF screening of millimeter-wave power MMICs to customer specifications. The test software is modular, making it easily adaptable to unique customer requirements and is **attached** to a **linked** database for rapid data analysis and **chip** delivery. A principal feature of the system is its sophisticated network of failure flags which are used to highlight potential processing/design problems. The flags are **linked** to a series of diagnostic tests performed on every MMIC in addition to the usual RF measurements such as power output, gain and **drain/gate** current. The diagnostic tests screen out noncompliant MMICs before RF test, thereby minimizing test time. Pareto analyses are presented showing the utility of the flags in diagnosing specific processing problems.

L35 ANSWER 2 OF 46 INSPEC COPYRIGHT 2002 IEE
AN 1998:5902877 INSPEC DN B9806-2560X-004
TI Single electronics with metallic and semiconducting nanostructures.
AU Ahmed, H. (Cavendish Lab., Cambridge Univ., UK)
SO Microelectronic Engineering (March 1998) vol.41-42, p.15. 5 refs.
Doc. No.: S0167-9317(98)00005-7
Published by: Elsevier
Price: CCCC 0167-9317/98/$19.00
CODEN: MIENEF ISSN: 0167-9317
SICI: 0167-9317(199803)41/42L.15:SEWM;1-8
Conference: Micro- and Nano- Engineering 97. MNE International Conference on Micro- and Nanofabrication. Athens, Greece, 15-18 Sept 1997
DT Conference Article; Journal
TC Practical; Experimental
CY Netherlands
LA English
AB Single electronics requires fabrication of an isolated nanoscale island **linked** to external circuitry via tunnel junctions. Alternative techniques have been developed for lateral metallic single electron device fabrication. Metallic nanoscale clusters were deposited between closely-spaced source and **drain** electrodes; electron transport from source to **drain** shows clear Coulomb blockade. Side **gates** are used to make single electron transistor structures. A buried **gate** device offers device control with lower **gate** voltages than side-gated structures. Another metallic structure development was combined source/**drain** fabrication by EBL with

nanoislands formed by colloidal particle **attachment** or cluster deposition methods. Semiconductor based single electronics has advantages over metallic structures, as SETs can be **coupled** with conventional circuitry. GaAs is used to make fine wires with a side **gate**, and electron transport in this disordered system shows distinct Coulomb blockade. This structure has been used for a single electron memory and single electron logic. SOI nanoscale islands and tunnel junctions were formed by lithography or oxidation techniques to show Coulomb blockade. Another development was transport in heavily doped Si nanowires on SiO2 to show single electron charging which is strongly affected by **gate** action. With this structure, a compact single electron memory structure was devised which can be integrated with CMOS. Novel memory concepts where single electron charging effects are used are being proposed and the application of single electronics to extremely large scale integration (ELSI) is a distinct prospect.

L35 ANSWER 3 OF 46 INSPEC COPYRIGHT 2002 IEE
AN 1998:5833412 INSPEC DN B9803-2570D-028
TI A DC method for measuring all the **gate** capacitors in MOS devices with atto-farad resolution.
AU Manku, T.; MacEachern, L. (Dept. of Electr. & Comput. Eng., Waterloo Univ., Ont., Canada)
SO IEEE Transactions on Semiconductor Manufacturing (Feb. 1998) vol.11, no.1, p.141-5. 7 refs.
Doc. No.: S0894-6507(98)00325-X
Published by: IEEE
Price: CCCC 0894-6507/98/$10.00
CODEN: ITSMED ISSN: 0894-6507
SICI: 0894-6507(199802)11:1L.141:MMGC;1-H
Conference: 5th International Symposium on Semiconductor Manufacturing (ISSM'96).
DT Journal
TC Practical; Experimental
CY United States
LA English
AB In this paper we present a new methodology for measuring all the intrinsic **gate** capacitors (i.e., **gate**-source, **gate**-**drain**, and **gate**-bulk) in a MOS device using a DC measurement scheme. The structure consists of two matched MOSFET's, one of which has a reference capacitor **attached** to its **gate**. The test structure was fabricated and the results show a resolution in the atto-farads range. The test structures use charge **coupling** to measure the **gate** capacitors.

L35 ANSWER 4 OF 46 INSPEC COPYRIGHT 2002 IEE
AN 1997:5531441 INSPEC DN A9709-8280T-013; B9705-7230-011
TI New chemical sensor based on a MOS transistor with rear contacts and two flat surfaces.
AU Osorio-Saucedo, R.; Luna-Arredondo, E.J.; Calleja-Arriaga, W.; Reyes-Barranca, M.A. (Dept. of Electr. Eng., Centro de Investigacion y de Estudios Avanzados, IPN, Mexico City, Mexico)
SO Sensors and Actuators B (Chemical) (Dec. 1996) vol.B37, no.3, p.123-9. 12 refs.
Doc. No.: S0925-4005(96)01978-8
Published by: Elsevier
Price: CCCC 0925-4005/96/$15.00
CODEN: SABCEB ISSN: 0925-4005
SICI: 0925-4005(199612)B37:3L.123:CSBT;1-S
DT Journal

TC Practical
CY Switzerland
LA English
AB This paper describes how a new chemical sensor can be made based on an insulated-**gate** field-effect transistor with electric contacts for the source, substrate and **drain** over the lower surface of the silicon crystal and with both surfaces flat. These source and **drain** contacts are possible because a deep phosphorus diffusion is carried out simultaneously from both surfaces of the silicon **wafer** , with junction depths between 80 and 100 mu m, through a silicon **wafer** with a thickness between 160 and 200 mu m. With this deep diffusion, it is possible to **join** both surfaces electrically. The **mounting** and the seal that are proposed are very simple, so they can be easily developed at any laboratory. The advantage of this sensor is that it is a device with flat surfaces and back contacts for **drain** and source, avoiding very basic technologies with poor quality control. We believe that **mounting** and sealing this device will be more reliable. Common **microelectronics** and silicon power device technology are used for this sensor. This proposed technology is a possible option to get cheaper and better chemical sensors. The described sensor type may be used to measure pH. Other ions can be analysed with additional selective membranes. Some initial results from the development of this technology are also reported, which allow us to understand that with this new technology, high-quality chemical sensors can be produced.

L35 ANSWER 5 OF 46 INSPEC COPYRIGHT 2002 IEE
AN 1997:5520474 INSPEC DN B9704-2560S-014
TI P-contact MESFETs for high voltage mixed-mode RF-applications.
AU Wennekers, P.; Zdebel, P.; Wilson, M.; Bushey, T.; Bernhard, B. (Sector Technol./CPL, Motorola Inc., Tempe, AZ, USA)
SO 18th Annual GaAs IC Symposium. IEEE Gallium Arsenide Integrated Circuit Symposium. Technical Digest 1996 (Cat. No.96CH35964)
New York, NY, USA: IEEE, 1996. p.155-8 of xv+332 pp. 5 refs.
Conference: Orlando, FL, USA, 3-6 Nov 1996
Sponsor(s): IEEE Electron Devices Soc.; IEEE Microwave Theory & Techn. Soc
Price: CCCC 0 7803 3504 X/96/$5.00
ISBN: 0-7803-3504-X
DT Conference Article
TC Application; Experimental
CY United States
LA English
AB MESFETs with P-well operating at higher **drain** voltage generate holes by impact ionization. They charge the GaAs substrate, give rise to increased output conductance and **drain** current transients at low temperature and facilitate inter-device **coupling**. Draining the holes by a P+-contact, which is **attached** to the source as an integral part of the device structure, neutralizes the adverse impact of holes on device performance. The improved MESFET is utilized in the digital section of a single-pole-eight-throw RF switch with integrated decoder.

L35 ANSWER 6 OF 46 INSPEC COPYRIGHT 2002 IEE
AN 1996:5391627 INSPEC DN B9611-2560R-044
TI Inductive damage and the impact of RF power and magnetic field during MERIE processes.
AU Salah, A.; Awadelkarim, O.O. (Electron. Mater. & Process. Res. Lab., Pennsylvania State Univ., University Park, PA, USA); Chan, Y.D.; Werking, J.

SO 1996 1st International Symposium on Plasma Process-Induced Damage (IEEE Cat. No.96TH8142)
Editor(s): Cheung, K.P.; Nakamura, M.; Gabriel, C.T.
Sunnyvale, CA, USA: American Vacuum Soc, 1996. p.131-2 of i+237 pp. 0 refs.
Conference: Santa Clara, CA, USA, 13-14 May 1996
Sponsor(s): IEEE/Electron Devices Soc.; American Vacuum Soc.; Japanese Soc. Appl. Phys
ISBN: 0-9651577-0-9
DT Conference Article
TC Experimental
CY United States
LA English
AB Summary form only given. We report on a new form of process-induced damage to submicron MOS transistors caused by metal 1 plasma etching. This form of damage, herein referred to as "inductive damage", is suggested to arise from inductive **coupling** between interconnect circuitry and time-varying magnetic fields during plasma exposure. We demonstrate the occurrence of inductive damage through the use of specially designed test structures consisting of fuse-**attached** metal loops acting as inductive antennas and **connecting** the **gate** and substrate of n-channel and p-channel MOSFETs. The MOSFETs, with lightly doped **drains** and channel lengths of 0.25 mu m and 0.50 mu m, are fabricated on 200 mm p/p+ silicon **wafers** using a full CMOS process flow. The metal 1 etch step was carried out using a BCl3/N2/Cl2 plasma in a magnetically-enhanced reactive ion etching (MERIE) tool.

L35 ANSWER 7 OF 46 INSPEC COPYRIGHT 2002 IEE
AN 1996:5345381 INSPEC DN B9609-1265D-023; C9609-5320G-016
TI Effects of source bias on the programming characteristics of submicron EPROM/flash EEPROM.
AU Geun Sook Park (Dept. of Electr. Eng., Korea Adv. Inst. of Sci. & Technol., Seoul, South Korea); Jae Ho Lee; Keun Hyung Park
SO Journal of the Korean Institute of Telematics and Electronics (March 1996) vol.33A, no.3, p.107-16. 8 refs.
Published by: Korea Inst. Telematics & Electron
CODEN: CKNOEZ ISSN: 1016-135X
SICI: 1016-135X(199603)33A:3L.107:ESBP;1-A
DT Journal
TC Practical; Theoretical; Experimental
CY Korea, Democratic People's Republic of
LA Korean
AB Recently, the flash memory has been attracting attention in the world semiconductor market for potential application as mass storage devices. One of the most significant barriers to the downscaling of **stacked -gate** devices such as EPROMs and flash EEPROMs is the large subthreshold leakage in the unselected cells **connected** with the bit line of a selected cell in the array during programming. The large subthreshold leakage is mainly due to capacitive **coupling** between the floating **gates** of the unselected cells and the bit line of the selected cell. In this paper, a new programming method to reduce the **drain** turn-on leakage significantly in the unselected cells during programming has been studied, where a small positive voltage (0.25-0.75 V) is applied to the source during programming, unlike the conventional programming method in which the source is grounded. The results of PISCES simulations and electrical measurements for a standard EPROM with 0.35 mu m effective channel length and 1.0 mu m effective channel width show that the subthreshold leakage in unselected cells is significantly large when the source is grounded, whereas it is negligible

DT Conference Article
TC Practical; Experimental
CY United States
LA English
AB A 0.4- mu m **stacked gate** cell for a 64-Mb flash memory has been developed which has the symmetrical side wall diffusion self-aligned (SSW-DSA) structure. Using the proposed SSW-DSA cell with p+ pockets at both the **drain** and the source, an adequate punchthrough resistance to scale the **gate** length down to sub-half-micron has been obtained. It is also demonstrated that the **uniform** erasing scheme applying negative bias to the **gate** which is adopted for the SSW-DSA cell shows lower trapped charges after write/erase (W/E) cycles evaluated by a charge pumping technique, and results in better endurance and retention characteristics than nonuniform erasing schemes. This cell will enable the realization of a 64-Mb flash memory with single 5-V supply operation, 106 W/E endurance, and sector erasing scheme.

L35 ANSWER 12 OF 46 INSPEC COPYRIGHT 2002 IEE
AN 1991:3809302 INSPEC DN B91009654
TI A self-aligned inverse-T **gate** fully overlapped LDD device for sub-half micron CMOS.
AU Wen, D.S.; Hsu, C.C.-H.; Taur, Y.; Zicherman, D.S.; Wordeman, M.R.; Ning, T.H. (IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA)
SO International Electron Devices Meeting 1989. Technical Digest (Cat. No.89CH2637-7)
New York, NY, USA: IEEE, 1989. p.765-8 of 913 pp. 6 refs.
Conference: Washington, DC, USA, 3-6 Dec 1989
Sponsor(s): IEEE
Price: CCCC CH2637-7/89/0000/0765$01.00
DT Conference Article
TC New Development; Practical; Experimental
CY United States
LA English
AB A novel self-aligned technique for fabricating inverse-T **gate** fully overlapped LDD (FOLD) MOSFETs is proposed. The technique uses an oxide or TiN buffer layer sandwiched in a polysilicon **gate** **stack** to act as an RIE (reactive ion etching) etch stop. Both the oxide and TiN exhibit good etch selectivities with respect to polysilicon. Therefore, a controllable, **uniform** polysilicon finger can be obtained to form the inverse-T structure. A 0.35- mu m n-channel inverse-T **gate** MOSFET with fully overlapped LDD (lightly doped **drain**) design has been fabricated and characterized. It is found that the inverse-T LDD device preserves the performance of a non-LDD device while providing reliability improvement similar to that of a conventional LDD device. The inverse-T LDD device is suitable for high-performance, high-reliability sub-half-micron device applications.

L35 ANSWER 13 OF 46 INSPEC COPYRIGHT 2002 IEE
AN 1990:3696233 INSPEC DN B90054635; C90051840
TI **Stacked** capacitor in trench cell for 16M-DRAM.
AU Kusters, K.H.; DoThanh, L.; Stelz, F.X.; Kellner, W.-U.; Muhlhoff, H.M.; Muller, W. (Siemens AG, Munchen, West Germany)
SO ESSDERC '89. 19th European Solid State Devices Research Conference
Editor(s): Heuberger, A.; Ryssel, H.; Lange, P.
Berlin, West Germany: Springer-Verlag, 1989. p.907-10 of xxv+963 pp. 6 refs.
Conference: Berlin, West Germany, 11-14 Sept 1989
ISBN: 3-540-51000-1

DT Conference Article
TC Practical
CY Germany, Federal Republic of
LA English
AB A 16 Mbit DRAM cell based on a **stacked** capacitor (STC) in an isolated trench has been investigated. The storage node of the capacitor consists of an As doped poly Si spacer in the trench. The poly Si spacer is **connected** to source of the transfer **gate** by a buried trench contact. The 'STC in trench' cell allows trench to trench/ **active area** distances of 0.7 mu m. The oxide/nitride/oxide (ONO) dielectric (deff=9 nm) on the As doped poly Si spacer exhibits similar properties as ONO on an Si substrate. Using the reported 'STC in trench' process a 5.12 mu m2 DRAM cell (design rules: 0.7 mu m) has been fabricated.

L35 ANSWER 14 OF 46 INSPEC COPYRIGHT 2002 IEE
AN 1985:2513488 INSPEC DN B85050697
TI Fabrication of fully self-aligned **joint-gate** CMOS structures.
AU Robinson, A.L.; Antonaidis, D.A.; Maby, E.W. (Dept. of Electr. Eng. & Comput. Sci., MIT, Cambridge, MA, USA)
SO IEEE Transactions on Electron Devices (June 1985) vol.ED-32, no.6, p.1140-2. 6 refs.
Price: CCCC 0018-9383/85/0600-114$01.00
CODEN: IETDAI ISSN: 0018-9383
DT Journal
TC Practical; Experimental
CY United States
LA English
AB A six-mask process that yields **stacked** CMOS structures with the source and **drain** of both transistors self-aligned to a **joint-gate** electrode has been developed. The features that permit full self-alignment are an edge-defined silicon nitride filament used as an oxidation mask, and overlapping polysilicon handles used to form the top transistor **sources** and **drain regions**. The individual NMOS and PMOS transistors have been characterized and together are functional in **joint-gate** CMOS inverters.

L35 ANSWER 15 OF 46 INSPEC COPYRIGHT 2002 IEE
AN 1984:2273245 INSPEC DN B84036844
TI A flip-**chip** GaAs power FET with **gate** and **drain** via **connections**.
AU Camisa, R.L.; Taylor, G.; Reichert, W.; Cuomo, F.; Brown, R. (David Sarnoff Res. Center, RCA, Princeton, NJ, USA)
SO IEEE Electron Device Letters (April 1984) vol.EDL-5, no.4, p.118-20. 6 refs.
Price: CCCC 0741-3106/84/0400-0118$01.00
CODEN: EDLEDZ ISSN: 0741-3106
DT Journal
TC Application; New Development; Practical
CY United States
LA English
AB A new microwave device format that **combines** flip-**chip mounting** and via-**connection** technologies is described. This approach avoids many of the compromises that are inherent in conventional microwave monolithic circuits and will be particularly important in power applications. The authors review the rationale for this device format and describe a new method of forming via **connections**

through thick semi-insulating substrates using laser drilling. Preliminary discrete GaAs FETs have been fabricated and results have been obtained through 18 GHz. At 12 GHz, an output power of 308 mW, a 28-percent power-added efficiency, and a 4.5-dB gain have been achieved with a 0.6-mm-wide GaAs FET. Efficiencies as high as 31 per cent were achieved with these preliminary devices.

L35 ANSWER 16 OF 46 INSPEC COPYRIGHT 2002 IEE
AN 1981:1693571 INSPEC DN B81027626
TI Performance of dual-**gate** GaAs MESFETs as phase shifters.
AU Pengelly, R.S.; Suckling, C.W.; Turner, J.A. (Plessey Res. Caswell Ltd., Towcester, UK)
SO 1981 IEEE International Solid-State Circuits Conference. Digest of Papers New York, NY, USA: IEEE, 1981. p.142-3 of 296 pp. 3 refs.
Conference: New York, NY, USA, 18-20 Feb 1981
Sponsor(s): IEEE; Univ. Pennsylvania
DT Conference Article
TC Experimental
CY United States
LA English
AB Discusses experimental work in S-band, which has investigated the way in which the transmission phase of a gain-controlled dual-**gate** GaAs FET amplifier depends both on the properties of the active device, and on the nature of the matching circuits used in the amplifier. The performance of a circuit optimized for broad-band operation is described. The **circuit configuration** investigated consists of a grounded-source bare-**chip** device **mounted** on a 0.635 mm alumina substrate, with three 25.4 mm long 50 Omega lines **connected** to the two **gates** and the **drain** of the device with wire bonds. Tuning discs were used as variable matching elements. The input signal was applied to the first **gate**, and the output taken from the **drain**; the second **gate** was determined with a 50 Omega resistive load. **Gate** and **drain** bias voltages were applied through standard bias tees. If Vg2 is held at the turning point in the characteristics (approximately -2.16 V), then a certain degree of phase shift could be achieved with a minimal change in gain by adjusting Vg1 only.

L35 ANSWER 17 OF 46 INSPEC COPYRIGHT 2002 IEE
AN 1978:1146886 INSPEC DN B78006393; C78003699
TI Integral-hybrid photomatrix for optical memory systems.
AU Kashlatyi, R.E.; Koyhevnikova, A.M.; Kruglikov, S.V.; Telitsyn, N.A.; Figurovskii, E.A.; Klebnikova, G.I.; Yudina, L.P.
SO Avtometriya (March-April 1977) no.2, p.50-3. 3 refs.
CODEN: AVMEBI ISSN: 0320-7102
Translation in: Optoelectronics, Instrumentation and Data Processing. 3 refs.
CODEN: OIDPE4 ISSN: 8756-6990
DT Journal; Original Abstracted
TC Application; Practical
CY USSR; United States
LA Russian
AB The use of a simple photo-element is advocated, consisting of a photodiode and an MOST switch; the **gate** of the transistor is **connected** to a counting bus and its **drain** to an output bus. A prototype **chip** is described in which crystals of 2*2 capacity are **mounted** on a glass substrate to give a 16*16 element matrix; 294 internal and 35 external contacts are required. The matrix is based on a 1.25 mm step length with 0.5*0.5 mm photodiode

elements; its sensitivity is 2*10-11 J; its registration time is better than 1 mu s.

L35 ANSWER 18 OF 46 INSPEC COPYRIGHT 2002 IEE
AN 1972:355560 INSPEC DN C72006300
TI **Integrated circuit** read-only memory.
CS Nat. Cash Register Co
PI UK 1250599 20 Oct. 1971
AD 25 June 1970
PRAI USA 841760 15 July 1969
DT Patent
TC Practical
CY United Kingdom
LA English
AB The memory has a first assembly including an array of semiconductor elements, **mounted** adjacent to a second assembly including an insulating substrate and an array of conductive elements located at positions corresponding to selected positions of the elements in the first array and being separated from them by an insulator layer so as to form insulated **gate** FET's at the selected positions. Preferably the source electrodes of each row and the **drain** electrodes of each column of elements in the first array are **connected** to respective row and column switches.

L35 ANSWER 19 OF 46 INSPEC COPYRIGHT 2002 IEE
AN 1970:119888 INSPEC DN B70014342; C70005461
TI Temperature change measuring device.
AU Wooten, F.T.
CS Corning Glass Works
PI USA 3453887 8 July 1969
AD 8 Feb. 1967
PRAI USA 614599
DT Patent
CY United States
LA English
AB Describes a temperature change measuring device having a metal oxide semiconductor field effect transistor with a **wafer** of pyroelectric materials directly **mounted** on the **gate** electrode. A charge produced in the pyroelectric material due to a change in temperature controls the transistor **drain** current. A simple ammeter **connected** between the transistor source and **drain** electrodes may be used to determine a change in temperature.

L35 ANSWER 20 OF 46 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:302929 HCAPLUS
TI Characterisation of ALCVD Al2O3-ZrO2 nanolaminates, **link** between electrical and structural properties
AU Besling, W. F. A.; Young, E.; Conard, T.; Zhao, C.; Carter, R.; Vandervorst, W.; Caymax, M.; De Gendt, S.; Heyns, M.; Maes, J.; Tuominen, M.; Haukka, Suvi
CS Philips Research Leuven, Kapeldreef 75, Louvain, B-3001, Belg.
SO Journal of Non-Crystalline Solids (2002), 303(1), 123-133
CODEN: JNCSBJ; ISSN: 0022-3093
PB Elsevier Science B.V.
DT Journal
LA English
AB Al2O3 and ZrO2 mixts. for **gate** dielecs. have been investigated as replacements for silicon dioxide aiming to reduce the **gate** leakage current and reliability in future CMOS devices. Al2O3 and ZrO2

films were deposited by at. layer chem. vapor deposition (ALCVD) on HF dipped silicon **wafers**. The growth behavior has been characterized structurally and elec. ALCVD growth of ZrO2 on a hydrogen terminated silicon surface yields films with deteriorated elec. properties due to the uncontrolled formation of interfacial oxide while decent interfaces are obtained in the case of Al2O3. Another concern with respect to reliability aspects is the relatively low crystn. temp. of amorphous high-k materials deposited by ALCVD. In order to maintain the amorphous structure at high temps. needed for dopant activation in the **source drain regions** of CMOS devices, binary Al/Zr compds. and laminated **stacks** of thin Al2O3 and ZrO2 films were deposited. X-ray diffraction and transmission electron microscope anal. show that the crystn. temp. can be increased dramatically by using a mixed oxide approach. Elec. characterization shows orders of leakage current redn. at 1.1-1.7 nm of equiv. oxide thickness. The permittivity of the deposited films is detd. by combining quantum mech. cor. capacitance voltage measurements with structural anal. by transmission electron microscope, X-ray reflectivity, Rutherford backscattering, XPS, and inductively **coupled** plasma optical emission spectroscopy. The k-values are discussed with respect to formation of interfacial oxide and possible silicate formation.

L35 ANSWER 21 OF 46 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:11149 HCAPLUS
TI Simple **stack** cell capacitor formation
IN Ukita, Shigenari; Anderson, Andrew A.; Niuya, Takayuki
PA USA
SO U.S. Pat. Appl. Publ., Division of Ser. No. US 1999-237084, filed on 25 Jan 1999 which
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2002001902	A1	20020103	US 2001-925200	20010809
PRAI US 1998-72786P	P	19980127		
US 1999-237084	A3	19990125		

AB A structure and method for fabricating an **integrated circuit** crown structure for use in a DRAM cell on a substrate comprising a common **source/drain region** (18) disposed within a substrate (12), the common **source/drain region** (18) **connected** to a bitline (22), a **gate** oxide (28) disposed over the common **source/drain region** (18) and forming at least two wordline **gates** (30), at least two storage node source/**drains** (20) adjacent to said **gates** (30) and contacted by storage node contacts (38) and a storage node bowl (36), the bowl being formed within adjacent supporting layers formed over said wordline **gates** wherein the storage node bowl (36) is formed, and electrically isolated from, the bitline (22) without being exposed to etching agents during its formation and without forming a wine glass stem structure and a crown extending from the top of the storage node bowl (36), is disclosed.

L35 ANSWER 22 OF 46 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:780520 HCAPLUS
DN 135:312226
TI Vertical transistor DRAM cell with **stacked** storage capacitor and associated method cell

IN Choi, Seungmoo
PA Agere Systems Guardian Corporation, USA
SO Eur. Pat. Appl., 18 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1148552	A2	20011024	EP 2001-303617	20010420
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 2001308203	A2	20011102	JP 2001-122417	20010420
PRAI	US 2000-553868	A	20000420		

AB An **integrated circuit** memory device includes a substrate having at least one **connection** line therein and a plurality of memory cells formed on the substrate. Each memory cell includes a pillar comprising a lower **source/drain region** for a cell access transistor elec. **connected** to the **connection** line, an upper **source/drain region** for the cell access transistor, and at least one channel region extending vertically between the lower and upper **source/drain regions**. Each memory cell further includes at least one lower dielec. layer vertically adjacent the substrate and laterally adjacent the pillar and at least one upper dielec. layer vertically spaced above the at least one lower dielec. layer and laterally adjacent the pillar. Further, each memory cell includes at least one **gate** for the at least one channel of the cell access transistor between the lower and upper dielec. layers so that the vertical spacing therebetween defines a **gate** length for the cell access transistor. A storage capacitor is also included in each memory cell adjacent the upper **source/drain region** of the cell access transistor and is elec. **connected** thereto.

L35 ANSWER 23 OF 46 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:347363 HCAPLUS
TI Semiconductor module
IN Nagase, Toshiaki
PA Kabushiki Kaisha Toyoda Jidoshokki Seisakusho, Japan
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6232654	B1	20010515	US 1999-349373	19990708
PRAI	JP 1998-195974	A	19980710		

AB A semiconductor module includes a MOSFET **chip** and a package for accommodating the MOSFET **chip**. The **drain** area of the MOSFET **chip** is **connected** to a base substrate. A source and a **gate** electrode are arranged on the top of the package, and also a **drain** electrode to be **connected** to the base substrate is arranged. On a printed-circuit board, to which a protection circuit is implemented, holes corresponding to the **drain** electrode, the source electrode, and the **gate** electrode are formed. The protection circuit is **attached** to the semiconductor module while the electrodes penetrate into the respective holes.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 24 OF 46 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:802375 HCAPLUS
DN 133:343488
TI Method for forming self-aligned selective silicide layer using chemical mechanical polishing in merged DRAM logic
IN Hwang, In-Seak
PA Samsung Electronics Co., Ltd., S. Korea
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6146994	A	20001114	US 1999-298904	19990426
	KR 2000005581	A	20000125	KR 1999-3756	19990204
PRAI	KR 1998-21065	A	19980608		
	KR 1999-3756	A	19990204		

AB A semiconductor device including a 1st area where a silicide layer is formed only on a **gate** electrode, and a 2nd area where a silicide layer is formed both on the **gate** electrode and on **source** and **drain areas** is produced by a method wherein a polishing stopper and an oxide layer are sequentially **stacked**, the **gate** electrode is exposed in a self-aligned manner, and then a 1st silicide layer is formed to thereby suppress misalignment in the process of manufg. a semiconductor device having a fine linear width. In the 1st area, when 1st and 2nd insulating layers are **stacked** and contact holes are formed directly **connected** to the semiconductor substrate, a 2nd silicide layer is formed at the bottoms of the contact holes, to reduce contact resistance and leakage current.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 25 OF 46 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:752153 HCAPLUS
DN 133:304524
TI High performance direct **coupled** FET memory cell
IN Bertin, Claude L.; Cronin, John E.; Hedberg, Erik L.; Mandelman, Jack A.
PA International Business Machines Corporation, USA
SO U.S., 42 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6137129	A	20001024	US 1998-2825	19980105

AB A pair of directly **coupled** field effect transistors (FETs), a latch of directly **coupled** FETS, a static random access memory (SRAM) cell including a latch of directly **coupled** FETs and the process of forming the directly **coupled** FET structure, latch and SRAM cell. The vertical FETs, which may be both PFETs, NFETs or one of each, are epi-grown NPN or PNP **stacks** sepd. by a **gate** oxide SiO2. Each device's **gate** is the source or **drain** of the other device of the pair. The preferred embodiment latch includes two such pairs of directly **coupled** vertical FETs

connected together to form cross **coupled** inverters. A pass **gate** layer is bonded to one surface of a layer of preferred embodiment latches to form an array of preferred embodiment SRAM cells. The SRAM cell may include one or two pass **gates**. The preferred embodiment SRAM process has three major steps. First, preferred embodiment latches are formed in an oxide layer on a silicon **wafer** . Second, the cell pass **gates** are formed on a pass **gate** or Input/Output (I/O) layer. Third, the I/O layer is bonded to and **connected** to the preferred latch layer.

RE.CNT 26 THERE ARE 26 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 26 OF 46 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:739803 HCAPLUS
TI Semiconductor device. [Machine Translation].
IN Edo, Yukiko
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000294735	A2	20001020	JP 1999-98186	19990405

AB [Machine Translation of Descriptors]. Capacity of the input/output terminal of the semiconductor device which operates at high speed the semiconductor device which easily can manage and can adjust is offered. Pin 101 outside the device is **connected** by the **gate** terminal of N channel MOS transistor 104 for capacity revision by aluminum wiring 106, the **drain** and the source of MOS transistor 104 as is **connected** mutually, are **connected** to bonding pad 105 by aluminum wiring 107. As for bonding pad 105, when the semiconductor **integrated circuit** device has been **mounted** on the package of the CSP and the like, doing the bonding is arranged in the possible site, MOS transistor 104 is formed with the process which is identical with the MOS transistor which forms the other internal circuit of the semiconductor **integrated circuit** device.

L35 ANSWER 27 OF 46 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:687704 HCAPLUS
TI Electric field effect transistor tip/**chip** and its packaging method. [Machine Translation].
IN Tanaka, Naoya; Yokoyama, Eiji; Aoyama, Naoki
PA Rohm Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000269260	A2	20000929	JP 1999-69938	19990316
	CN 1267911	A	20000927	CN 2000-102989	20000314
	CN 1267911	A	20000927	CN 2000-102989	20000314
PRAI	JP 1999-69938	A	19990316		

AB [Machine Translation of Descriptors]. The electric field effect transistor tip/**chip** which can decrease production cost and **mounted** cost is offered. Made 2 electric field effect transistors

in 1 electric field effect transistor tip/**chip** and 1 was packed, the source and the **drain** of each electric field effect transistor made the principal plane 1 A of one side of electric field effect transistor tip/**chip** face, 1 in on one hand principal plane 1 A, the **gate** padding 2 which continues in the saw spud 3 which continues in the source, 5 and the **gate** and 4, formed individually in every each electric field effect transistor, made the **drain** of each electric field effect transistor the other principal plane of electric field effect transistor tip/**chip** face, 1 in the other principal plane, the formation it did the electric conductor membrane 6 which **connects** the **drain** of each electric field effect transistor mutually.

L35 ANSWER 28 OF 46 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:636234 HCAPLUS
DN 133:216531
TI Fabrication of transistor with integrated poly/metal **gate** electrode
IN Gardner, Mark I.; Wristers, Derick J.; Cheek, Jon D.
PA Advanced Micro Devices, Inc., USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6118163	A	20000912	US 1998-17720	19980204
	US 5994193	A	19991130	US 1998-95088	19980610
PRAI	US 1998-17720	A3	19980204		

AB An **integrated circuit** transistor and method of making the same are provided. The transistor includes a substrate, first and second **source/drain regions**, and a **gate** electrode **stack coupled** to the substrate. The **gate** electrode **stack** is fabricated by forming a first insulating layer on the substrate, forming a first conductor layer on the first insulating layer, and forming a metal layer on the first conductor layer. A second insulating layer, such as an interlevel dielec. layer, is **coupled** to the substrate adjacent to the **gate** electrode **stack**. Sidewall spacers and LDD processing may be incorporated. The transistor and method integrate metal and polysilicon into a self-aligned **gate** electrode **stack**.
RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 29 OF 46 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:378148 HCAPLUS
DN 132:355709
TI Flash memory structure and method of manufacture
IN Hong, Gary
PA United Semiconductor Corp., Taiwan
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6071776	A	20000606	US 1998-186748	19981105

	TW 400609	B	20000801	TW 1998-87112801	19980804
	US 6281544	B1	20010828	US 2000-521984	20000309
PRAI	TW 1998-87112801	A	19980804		
	US 1998-186748	A3	19981105		

AB A method is claimed of manufg. a flash memory structure that also includes the process of forming a shallow trench isolation structure. The method comprises the steps of providing a semiconductor substrate, and then forming a shallow trench isolation structure within the substrate. Thereafter, etching is carried out to form a shallow trench within a portion of the shallow trench isolation structure. The shallow trench is formed where a common source terminal is subsequently formed. Next, metallic material is deposited into the trench to form a buried metallic layer. Then, a **stacked gate** is formed above the semiconductor substrate. Finally, ions are implanted into the substrate on each side of the **stacked gate** using the **stacked gate** itself as a mask to form a **source region** and a **drain** region. The **source region** and the buried metallic layer are **connected** together to form a common **source region**. The process of forming the buried metallic layer in the substrate not only is compatible with the process of forming a shallow trench isolation structure, but the device so formed also takes up less **chip** area. Hence, a device array having a higher d. can be produced.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 30 OF 46 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:314128 HCAPLUS
TI Semiconductor **integrated circuit** device. [Machine Translation].
IN Hyodo, Kimihiro
PA Sharp Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000132999	A2	20000512	JP 1998-308551	19981029

AB [Machine Translation of Descriptors]. In the semiconductor **integrated circuit** device of nonvolatile memory built-in, until recently with technology the Change-over Switch of the external which is necessary is made unnecessary, reduction of number of articles and improvement of **mounted** efficiency are assured. Provides with the terminal state means for switching which change the state of the above-mentioned Test/vpp terminal according to the Savpp signal which is outputted from the Vpp inspection circuit 2 which checks the high tension which is inputted into Test/vpp terminal 3 and said inspection circuit. Said terminal state means for switching, the SAVPP signal from above-mentioned inspection circuit, through invertor 4, are inputted by that **gate**, the source is **connected** by **connection** matrix voltage, furthermore, that **drain** through pull-down resistant R1, is constituted by the N channel Mos transistor Q 1 which is **connected** to the above-mentioned Test/vpp terminal.

L35 ANSWER 31 OF 46 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:260390 HCAPLUS

DN 132:355492
TI An ISFET based chemical sensor for the food industry
AU Corra, M.; Pignatel, G. U.; Conci, P.; Margesin, B.; Zen, M.; Maglione, A.
CS Lab. ElettroOttica, Lab. ElettroOttica, Facolta di Ingegneria dell' Universita, Trento, 38050, Italy
SO Sensors and Microsystems, Proceedings of the Italian Conference, 4th, Roma, Feb. 3-5, 1999 (2000), Meeting Date 1999, 241-246. Editor(s): Di Natale, Corrado; D'Amico, Arnaldo; Davide, Fabrizio. Publisher: World Scientific Publishing Co. Pte. Ltd., Singapore, Singapore.
CODEN: 68UUAK
DT Conference
LA English
AB Silicon integrated ISFET (Ion Sensitive Field Effect Transistor) is widely used as pH sensor of electrolytic solns., and by adding properly designed membranes on top of the chem. sensitive **gate** area a variety of chems. of interest for the food industry can be detected. The main remaining problems to be solved for a wide acceptance of this type of sensor are the need of a ref. electrode, which contains dangerous and poisonous chems., like KCl and Ag/AgCl, and the development of esp. designed, bio-compatible packages. Finally, an efficient protection of the **gate** area with respect to ESD (Electro-Static Discharge) is required to assure the sensor long term reliability. In our sensor prototype a double ISFET **chip** has been designed and fabricated at IRST by a dedicated fabrication process. The use of two nominally identical ISFET transducers, one exposed to the electrolyte under testing and the other exposed to a suitably selected ref. soln. allows a differential read-out of the output signal, thus avoiding the need of the ref. electrode. The differential read-out also eliminates or drastically reduces all the problems related to the sensor **drift**, common mode noise and temp. fluctuations. A specially designed stainless steel package which completely covers the conventional plastic encapsulation is being used to assume a food bio-compatibility. A dedicated PCB **mounted** read-out electronics has been developed, which includes a const. voltage, const. current bias circuit, A/D conversion, micro-controller, data anal. and output signal display. The ISFET sensor is **coupled** with a Pt100 for simultaneous measurement of pH and temp. The prototype electrochem. characteristics and the results of preliminary tests on the field will be reported.
RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L35 ANSWER 32 OF 46 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:33326 HCAPLUS
TI The circuit device which the transistor tip/**chip** and the transistor tip/**chip** the loading is done. [Machine Translation].
IN Okamoto, Yasuhiro
PA Nec Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2000012562	A2	20000114	JP 1998-173699	19980619

AB [Machine Translation of Descriptors]. Lose wiring by the wire to the **gate** electrode and the **drain** electrode, at the same time easily try to be able visual examn. after **mounting**. The invention which the disclosure is done related to the transistor tip/

chip 202 A where, the source electrodes and the **gate** electrode and the **drain** electrode were formed on the surface of the semiconductor substrate 21 which is chipped was formed to the back of transistor tip/**chip** 202 A, was formed to the back of source withdrawal electrode 23 A and the transistor tip/**chip** 202 A which the source electrodes are **connected**, was formed to the back of **gate** withdrawal electrode 26 D and the transistor tip/**chip** 202 A which the **gate** electrode are **connected**, possessing with the **drain** withdrawal electrode 28 D which, the **drain** electrode is **connected** it becomes.

L35 ANSWER 33 OF 46 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:781934 HCAPLUS
DN 132:17946
TI Semiconductor memory device with SOI (silicon-on-insulator) structure, and method for its fabrication
IN Kim, Yung-Gi
PA Samsung Electronics Co. Ltd., S. Korea
SO Ger. Offen., 10 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 19923388	A1	19991202	DE 1999-19923388	19990521
	TW 413943	B	20001201	TW 1999-88105357	19990403
	GB 2337851	A1	19991201	GB 1999-9584	19990426
	GB 2337851	B2	20000823		
	FR 2779273	A1	19991203	FR 1999-6620	19990526
	JP 11354756	A2	19991224	JP 1999-147194	19990526
	US 2002001913	A1	20020103	US 2001-934761	20010823
PRAI	KR 1998-19164	A	19980527		
	US 1999-320214	A3	19990526		

AB A silicon-on-isolator transistor with a **gate** electrode, a **source/drain area** and a channel area, is elec. **connected** with a conductor through an opening in a insulating layer that is formed between them. The presence of the conductor prevents any irregular variation in the threshold potential and diminishes the loss underneath the threshold and accordingly guarantees a high working speed. A transistor with a **source/drain area** and a channel area is formed on a surface of a semiconductor substrate. A first insulating layer is formed on the transistor covering the semiconductor substrate. A handling **chip** is **attached** to the first insulating layer. The other surface of the semiconductor is ground and polished. A second insulating layer is formed on the polished semiconductor substrate. A conductor is formed on the second insulating layer and elec. **connected** to the channel area of the transistor through the second insulating layer.

L35 ANSWER 35 OF 46 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:748716 HCAPLUS
TI **Integrated circuit** with at least one transistor and a capacitor and corresponding production method
IN Hofmann, Franz; Krautschneider, Wolfgang
PA Siemens Aktiengesellschaft, Germany
SO PCT Int. Appl.
CODEN: PIXXD2
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9960608	A2	19991125	WO 1999-DE1501	19990519
	W: JP, KR, US				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	TW 428313	B	20010401	TW 1999-88107961	19990517
	EP 1097471	A1	20010509	EP 1999-936280	19990519
	R: DE				
PRAI	DE 1998-19822500	A	19980519		
	WO 1999-DE1501	W	19990519		

AB A structured conductive layer (L) and a structure, by means of which the transistor can be controlled, e.g. a word line (W), are arranged on top of each other. A vertical conductive structure (S), e.g. a spacer, **connects** a first **source/drain zone** (S/D1) of the transistor to the conductive layer (L), both of which form a first capacitor electrode having a large effective surface with higher packing density. A capacitor dielectric (KD) and a second capacitor electrode (P2) placed on top thereof are arranged above the vertical conductive structure (S) and the conductive layer (L). The transistor can be a vertical transistor. The vertical conductive structure (S) can be arranged on a first flank (F1) of the first **source/drain**

zone (S/D1) and a **gate** electrode of the transistor can be **mounted** on a bordering second flank of the **source/drain zone** (S/D1). The circuit can be a DRAM cell array in which channel stop structures are arranged on the first flank of the first trenches, **gate** electrodes are arranged on the second flanks of the first trenches and vertical conductive structures are arranged on the second trenches (G2) and in which the word lines (W) extend between the second trenches (G2).

L35 ANSWER 36 OF 46 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:15670 HCAPLUS
DN 128:96448
TI Making a buried interconnection structure
IN Padmanabhan, Gobi R.
PA LSI Logic Corp., USA
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5702957	A	19971230	US 1996-710783	19960920

AB Disclosed is an **IC** structure providing conductive lines for routing within a semiconductor substrate immediately below the level of the active **IC** devices. These buried conductive lines are insulated from each other by dielec. regions formed as an insulating plane immediately below the active devices and resembling a conventional Si-on-insulator (SOI) structure. Within this plane, however, the buried conductive lines provide routes between various active device elements to form some circuit **connections** such as intracell **connections** for a **gate** array. Thus, the buried conductive lines replace some routing from the metalization/dielec. layer **stack** on top of the **active region**.

L35 ANSWER 37 OF 46 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:317177 HCAPLUS
DN 127:43005
TI Monolithic integration of GaAs optoelectronic devices using thermal oxide isolation (TOI)
AU Wheeler, C. B.; Daryanani, S.; Shen, J.; Zhang, Y. -H.
CS Department of Electrical Engineering, Center for Solid State Electronics Research, Arizona State University, Tempe, AZ, 85287-5706, USA
SO Proc. SPIE-Int. Soc. Opt. Eng. (1997), 3003(Vertical-Cavity Surface-Emitting Lasers), 75-84
CODEN: PSISDG; ISSN: 0277-786X
PB SPIE-The International Society for Optical Engineering
DT Journal
LA English
AB A novel integration method is described that relies on the thermal oxidn. of AlAs to form a buried current blocking layer. This integration technol., called thermal oxidn. isolation (TOI), is an extension of recent work involving oxidized vertical-cavity surface-emitting lasers (VCSELs). However, in addn. to incorporating a conventional thermal oxide current aperture to define VCSEL **active regions**, a buried oxide layer is also used to provide inter-device isolation. As a demonstration of this concept, a GaAs MESFET and resonant cavity LED are integrated and characterized. The buried oxide layer is situated under the FET channel such that the transistor is effectively **stacked**

on top of the LED. The oxide layer is also used to form a current aperture in the LED and directs current flow vertically through this device. Solid-source MBE is used to grow the device layers on a p-type GaAs substrate. The epitaxial structure consists of a p-type bottom mirror consisting of 24.5 pairs of alternating AlAs and GaAs quarterwave layers, an undoped one-wave **active region** contg. 3 .times. 80 .ANG. InGaAs quantum wells and a single n-type AlAs/GaAs top mirror period. The fabrication sequence, described in some detail, is straightforward. A wet etch is used to define one mesa for the LED and a second for the MESFET. The top AlAs layer, exposed at the mesa periphery by this etch, is oxidized at 410.degree.C in a steam ambient to form the current-guiding regions. A conventional MESFET fabrication sequence is then used to complete the transistor and form the LED cathode (which is **connected** to the FET **drain**). A back contact is then deposited to form the LED anode. In all, five mask levels are used to fabricate the integrated FET/LED (or VCSEL) structure. Functionality of these prototype devices is demonstrated by dc and modulation measurements. The MESFET **gate** length and width are 3 .mu.m and 100 .mu.m, resp. The transistor operated in the depletion mode with a typical Idss of 8 mA and a max. transconductance of 35 mS/mm. The LED wavelength is about 990 nm and has output power in the .mu.W range when driven by the MESFET.

L35 ANSWER 38 OF 46 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:178690 HCAPLUS
DN 126:179921
TI Flip-**chip** semiconductor devices
IN Kamimura, Kazuyoshi; Nashimoto, Yasunobu; Kozu, Hideaki
PA Nippon Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 09008060	A2	19970110	JP 1995-150466	19950616

AB Semiconductor **chips**, in which field-effect transistor elements are formed by positioning source, **gate**, and **drain** electrodes on semiconductor substrates, and .gtoreq.2 of the source (or **drain**) electrodes are mutually **connected** through air bridges (e.g., Au), are **mounted** on media with the bridges adhered or hot pressed to the **mount** surface of the media.

L35 ANSWER 39 OF 46 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:592667 HCAPLUS
DN 121:192667
TI Charge buildup damage to **gate** oxide
AU Gabriel, Calvin
CS VLSI Technol., Inc., San Jose, CA, 95131, USA
SO Proc. SPIE-Int. Soc. Opt. Eng. (1994), 2091(Microelectronic Processes, Sensors, and Controls), 239-47
CODEN: PSISDG; ISSN: 0277-786X
DT Journal
LA English
AB "Antenna" structures over thick oxide were used to detect charge buildup damage to **gate** oxide, and **gate** leakage was measured to characterize the extent of damage. Polycide, metal 1, and metal 3 antennas with both area-intensive and edge-intensive configurations were

included. After processing through a full triple-level metal, 135 .ANG. **gate** oxide, 0.6 .mu.m CMOS flow, individual 5 .times. 1 .mu.m transistors (over **gate** oxide which had been stressed by the charge collected through an **attached** antenna during **wafer** fabrication) were measured and considered damaged if a current > 1 nA leaked through the oxide when a 5.5 V stress was applied to the **gate** during testing. There was a monotonic increase in failures with antenna area ratio for the polycide antenna, beginning at a polycide antenna:**gate** oxide area ratio of about 1000:1. The polycide antennas showed a further trend with antenna edge ratio, defined as the ratio of antenna edge length (where the antenna was designed with polycide fingers) to **gate** oxide area. Increasing the antenna edge ratio caused an increase in leakage failure even when the antenna area ratio was not increased. Clearly, one or more fabrication steps caused charge buildup on the polycide antennas through both the top surface and through the edges. Several processes could be causing the charge buildup, including ashing, polycide etching, LDD or source/**drain** junction implantation, spacer etching, or contact etching. A series of expts. was conducted varying process or equipment used at several etching or ashing steps to det. the source of this charge buildup. Several of these steps are shown to be capable of causing oxide damage. **Gate** leakage failures were mapped to det. if there were patterns to the failure. Failures were **uniform** in some cases, and in others the failures were concd. at the center or the edges of the **wafers**. In contrast to the charge buildup occurring on the polycide antennas, there was little evidence of charge buildup occurring on metal 1 or metal 3 antennas, even for area ratios as high as 100,000:1 or edge ratios as high as 40,000:1.

L35 ANSWER 40 OF 46 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:418838 HCAPLUS
DN 119:18838
TI Manufacture of semiconductor **integrated circuits**
IN Ota, Hiroyuki
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04348567	A2	19921203	JP 1991-120618	19910527
	JP 3104285	B2	20001030		

AB The title method comprises: (1) successive **pile** up of a 1st antioxidative insulating film and a 2nd insulating film on a polycryst. Si layer which was formed on a **gate** oxidative film on a 1st cond.-type semiconductor substrate, (2) selectively etching the two insulating films and the polycryst. Si layer to form a **gate** electrode, (3) forming an oxide film on the side of the **gate** electrode and on the substrate by thermal oxidn. using the 2nd insulating film as a mask, (4) forming a **source drain region** by impurity ion implantation of a 2nd cond.-type using the **gate** electrode as a mask, (5) forming a contact hole on the **source drain region** by entire etch back, and (6) piling up a conductor layer on the entire surface including the contact hole and then patterns to form a wiring to **connect** with the **source drain region**. Compared with conventional processes, the method of the invention can reduce the area

FILE 'WPIX, JAPIO' ENTERED AT 11:21:49 ON 30 APR 2002
L1 846742 S IC OR ICS OR ((INTEGRATED OR LOGIC)(W)(CIRCUIT)) OR (MICRO)(W)(CIRCUIT OR CHIP OR ELECTRONIC?) OR CHIP OR MICROCIRCUIT OR DIE OR LOGIC(W) CIRCUIT OR WAFER OR MICROELECTRONIC? OR (CIRCUIT OR LOGIC)(W)(CONFIGURATION)
L2 5778762 S STACK### OR MOUNT? OR PILE OR PILED OR MOUND? OR ATTACH? OR FASTEN? OR AFFIX? OR CONNECT? OR JOIN? OR LINK? OR COUPL?
L3 4559538 S CONNECT? OR JOIN### OR COMBINE OR CONJOIN? OR CONJUGATE OR CONSOLIDATE OR COUPL? OR LINK### OR UNIF### OR UNITE OR YOKE
L4 238966 S DRAIN OR DRIFT OR (ACTIVE OR DIFFUSION OR SOURCE)(2N)(REGION OR REGIONS OR AREAS OR AREA OR ZONE OR ZONES)
L5 39727 S LEADFRAME OR LEAD(2N) FRAME
L6 24153 S L1 AND L4
L7 11985 S L6 AND L2
L8 80 S L7 AND L5
L9 75 S L8 AND L3
L10 4 S L9 AND (WINDOW OR OPEN?)
L11 16 S L9 AND (POSTS OR SPHERE OR SPHERES OR BALL OR PLATE OR BUMP?)
L12 16 S L11 NOT L10
L13 32 S L9 AND (GATE OR GATES OR THYRISTOR OR LOGIC(2N) ELEMENT)
L14 21 S L13 NOT (L10 OR L12)
L15 2 S L9 AND (LEAD(2N) RAIL)
L16 0 S L15 NOT ((L10 OR L11 OR L12 OR L13 OR L14))
L17 3 S L7 AND (LEAD(2N) RAIL)
L18 1 S L17 NOT ((L10 OR L11 OR L12 OR L13 OR L14))

L19 18826 S L1 AND L5
L20 11941 S L19 AND L2
L21 690 S L19 AND (GATE OR GATES OR THYRISTOR OR LOGIC(2N) ELEMENT)
L22 37 S L21 AND L4
L23 451 S L20 AND (GATE OR GATES OR THYRISTOR OR LOGIC(2N) ELEMENT)
L24 33 S L23 AND L4
L25 1 S L24 NOT ((L10 OR L11 OR L12 OR L13 OR L14 OR L15 OR L16 OR L17 OR L18))
L26 4 S L22 NOT ((L10 OR L11 OR L12 OR L13 OR L14 OR L15 OR L16 OR L17 OR L18) OR L25)
L27 2 S L9 AND CLIP

L28 0 S L27 NOT ((L10 OR L11 OR L12 OR L13 OR L14 OR L15 OR L16 OR L17 OR L18) OR L25 OR L26)
L29 21601 S L2 AND L5
L30 11941 S L29 AND L1
L31 34 S L9 NOT ((L10 OR L11 OR L12 OR L13 OR L14 OR L15 OR L16 OR L17 OR L18) OR (L25 OR L26 OR L27))

L12 ANSWER 1 OF 16 WPIX (C) 2002 THOMSON DERWENT
AN 2002-199526 [26] WPIX
DNN N2002-151654
TI Flip-**chip** MOSFET manufacturing method involves arranging copper clip to backside of **die** using solder paste so that copper clip contacts **drain** area of **die** and lead rail.
DC U11
PA (FAIH) FAIRCHILD SEMICONDUCTOR CORP
CYC 1
PI JP 2001351941 A 20011221 (200226)* 6p
ADT JP 2001351941 A JP 2001-114665 20010412
PRAI US 2000-548946 20000413
AB JP2001351941 A UPAB: 20020424
NOVELTY - A **die** (15) having several solder **bumps** is arranged on **lead frame** (11) such that solder **bumps** contact source and gate **connection** of the **lead frame**. A copper clip (16) is arranged to back side of **die** using solder paste, so that copper clip contacts with **drain** area of **die** and lead rail. Solder paste and solder **bump** are reflowed.
USE - For manufacturing flip-**chip** type MOSFET.
ADVANTAGE - **Die** with **bump** is **attached** to **chip** device directly and **attachment** using clip to **die** is easily enabled.
DESCRIPTION OF DRAWING(S) - The figure shows a perspective diagram of flip-**chip** MOSFET device.
Lead frame 11
Die 15
Copper clip 16
Dwg.1/5

L12 ANSWER 2 OF 16 WPIX (C) 2002 THOMSON DERWENT
AN 2001-601011 [68] WPIX
DNN N2001-448247
TI Dual **lead frame** high voltage device package has leads whose inner leads directly **couples source/ drain region** and gate of **chip**, and packaging material to seal lead, **chip** and conductive **plate** by exposing outer leads.
DC U11
IN HUANG, C
PA (SITR-N) SITRON PRECISION CO LTD
CYC 1
PI US 6215176 B1 20010410 (200168)* 8p
ADT US 6215176 B1 US 1999-313171 19990517
PRAI TW 1999-107215 19990504
AB US 6215176 B UPAB: 20011121
NOVELTY - The inner leads (54,54') of the two leads (28,28') are respectively **coupled** to the **source/drain region** and gate of the **chip** (22). The surface (56) of conductive **plate** (29) is **coupled** to **chip** surface (25). The packaging material seals the **chip**, inner leads and conductive **plate** by exposing the outer leads (53,53') of lead.
DETAILED DESCRIPTION - The erose edges of the conductive **plate** dissipate stress generated by curing the packaging material for the sealing step. The leads (28,28') and the conductive **plate**

are **coupled** to the **source/drain region** and gate via the conductive material (24). The conductive **plate** erose edges are semicircular concave regions and the conductive material is silver paste.

USE - For e.g. dual **lead frame** high voltage device package.

ADVANTAGE - Since the lead and the conductive **plate** are directly **coupled** to the **chip**, the signal transmitting path is reduced and the resistance of the package is also reduced. The conductive **plate** serves as a heat slug to help to dissipate heat generated by operating the **chip**. Since the signal transmitting path is short, the impedance decreases and signal decay and delay do not occur.

DESCRIPTION OF DRAWING(S) - The figure shows schematic, cross sectional view of the dual **lead frame** package.

Chip 22
Conductive material 24
Chip surface 25
Leads 28,28',53,53',54,54'
Conductive **plate** 29
Conductive **plate** surface 56

Dwg.3/6

L12 ANSWER 3 OF 16 WPIX (C) 2002 THOMSON DERWENT
AN 2001-210208 [21] WPIX
DNN N2001-150109 DNC C2001-062375
TI Fabrication of a semiconductor **chip** scale package by providing a **chip** and conductive **plates**, filling an insulating material, removing the conductive **plate**, and performing a scribing process.
DC A85 L03 U11
IN HUANG, C; TSENG, S
PA (HUAN-I) HUANG C; (TSEN-I) TSENG S
CYC 2
PI US 6177719 B1 20010123 (200121)* 12p
TW 408411 A 20001011 (200121)
ADT US 6177719 B1 US 2000-478860 20000107; TW 408411 A TW 1999-105092 19990331
PRAI TW 1999-105092 19990331
AB US 6177719 B UPAB: 20010418

NOVELTY - A **chip** scale package (CSP) of semiconductor is fabricated by providing a **chip** having a first surface which includes a set-up of gate and first **source/drain region**, and a second surface which includes a set-up of second **source/drain region**; providing first and second conductive **plates**; filling an insulating material; removing the first conductive **plate**; and performing a scribing process.

DETAILED DESCRIPTION - Fabrication of a CSP of semiconductor comprises: providing a **chip** (40) having a first surface which includes a set-up of gate and first **source/drain region**, and a second surface which includes a set-up of second **source/drain region**; providing first and second conductive **plates** disposed on the first and the second surfaces of the **chip**, respectively; filling an insulating material between the **chip** and the substrate, and the **chip** and second conductive **plate**; removing the first conductive **plate** to expose a portion of the insulating material excluding that covered by the first and second **bumps** on the first surface; and performing a scribing process to expose a side surface

(72) of the first **bump**, the second **bump**, the second conductive **plate**, and the **chip**. The first conductive **plate** (64) comprises a substrate where first and second **bumps** are disposed on the same side to make the first **bump** and the gate, and the second **bump** (62) and the first **source/drain region** electrically **couple**, respectively by using a conductive bond (54).

USE - The method is used for fabricating CSP of semiconductor.

ADVANTAGE - The process is simple and low in cost because the conductive **plate** needs only a simple alignment and compression to **connect** to the electrodes of the **chip**, and the preparation of the conductive **plate** employs the process similar to that of the **lead frame** which is simple in structure. The CSP shortens the path of signal transmission to improve **chip** performance because the surfaces of the conductive block **connect** the electrodes of the **chip**, and the side surface of the conductive block is **connected** to the printed circuit board. It has a reduced volume because it employs the structure of **chip** level package.

DESCRIPTION OF DRAWING(S) - The figure is a schematic view of the CSP.

Chip 40

Conductive bond 54

Bump 62

Conductive **plate** 64

Plated layer 68

Side surface of the conductive block 72

Dwg.5/6

L12 ANSWER 4 OF 16 WPIX (C) 2002 THOMSON DERWENT
AN 2001-202068 [20] WPIX
DNN N2001-144094 DNC C2001-059940
TI Electroplating system for plating continuous articles, e.g. **lead frame** stock material, includes contact cell in which plating solution is integrated.
DC L03 M11 U11 X25
IN DREW, D M; MOEHLE, P R; SMITH, S J
PA (TEXI) TEXAS INSTR INC
CYC 1
PI US 6187166 B1 20010213 (200120)* 10p
ADT US 6187166 B1 Provisional US 1998-82474P 19980421, US 1999-294218 19990416
PRAI US 1998-82474P 19980421; US 1999-294218 19990416
AB US 6187166 B UPAB: 20010410

NOVELTY - An electroplating system includes a continuous electrical **connection** between the direct current power supply and a cathode (100) from a series of plating cells (410), via a rotating contact; and a contact cell (420) where the rotating contact is cooled by the plating solution (111) of the plating cells.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a process for electroplating a metal coating into a continuous article from a series of plating baths having the same or compatible plating solutions involving immersing the article in the plating solution, passing direct current to the article by way of a rotating contact, cooling the contact using plating solution, and transporting the article through each of the series of plating baths having the same composition using the same process for electrical contact and cooling.

USE - The system is used to **plate lead frame** stock material (claimed) such as those used in packaging **integrated circuits**. The produced **integrated**

L10 ANSWER 1 OF 4 WPIX (C) 2002 THOMSON DERWENT
AN 2001-655866 [75] WPIX
TI **Stacked chip** package.
DC U11
IN HWANG, S U
PA (SMSU) SAMSUNG ELECTRONICS CO LTD
CYC 1
PI KR 2001061886 A 20010707 (200175)* 1p
ADT KR 2001061886 A KR 1999-64436 19991229
PRAI KR 1999-64436 19991229
AB KR2001061886 A UPAB: 20011220
NOVELTY - A **stacked chip** package is provided to form a single package by **mounting** a plurality of semiconductor **chip** on a **lead frame**.
DETAILED DESCRIPTION - A **lead frame** has **chip-mounting** regions(21b,22b) and leads(21a,22a). Two or more semiconductor **chips**(11,13,15,17) are **mounted** on the **chip mounting** regions(21b,22b) of the **lead frame**. A bonding wire(25) **connects** electrically bonding pads(12,14,16,18) with the leads(21a,22a). The semiconductor **chips**(11,13,15,17) and the bonding wire(25) are covered by a package body(27). The bonding pads(12,14,16,18) are formed at edges of **active regions** of semiconductor **chips** (11,13,15,17). The semiconductor **chips**(11,13,15,17) are **stacked** to **open** the bonding pads(12,14,16,18). The semiconductor **chips**(11,13,15,17) are **mounted** on the **chip mounting** regions(21b,22b) of the **lead frame**.
Dwg.1/10

L10 ANSWER 2 OF 4 WPIX (C) 2002 THOMSON DERWENT
AN 1992-277700 [34] WPIX
DNN N1992-212387 DNC C1992-123552
TI Semiconductor pressure sensor in plastic moulded package - can be made with a lower strain level due to thermal expansion coefficient mismatch by careful optimisation of some dimensions.
DC A85 L03 S02 U11 U12
IN HIROSE, T; ICHIYAMA, H; TAKAHASHI, Y
PA (MITQ) MITSUBISHI DENKI KK; (MITQ) MITSUBISHI ELECTRIC CORP
CYC 4
PI DE 4203832 A 19920813 (199234)* 13p
JP 04258176 A 19920914 (199243) 6p
US 5207102 A 19930504 (199319) 13p
DE 4203832 C2 19960613 (199628) 14p
KR 9501169 B1 19950211 (199647)
ADT DE 4203832 A DE 1992-4203832 19920210; JP 04258176 A JP 1991-38902 19910212; US 5207102 A US 1991-763217 19910920; DE 4203832 C2 DE 1992-4203832 19920210; KR 9501169 B1 KR 1992-1454 19920131
PRAI JP 1991-38902 19910212
AB DE 4203832 A UPAB: 19931006
The semiconductor sensor consists of a pressure sensitive **die** (1) with a resistance (3) and featuring a membrane (2), a **chip** -contact plane (7) on which the **chip** support (5) is placed and bonded using an adhesive (6), pref. silicone rubber. The **chip** is **connected** via a contact area (4) and a bondwire (9) to a **leadframe** (8). An outer package (10), pref. of epoxy-resin, encapsulates the above parts except the **die** surface above the membrane (5) and the backside **chip** contact plane (7).

Optimisation requires a ratio of support (5) thickness and **chip** (1) thickness of 7.5 or less. The other major design parameter is the ratio of the **opening** in the top of the package and the width of the membrane area, which is pref. 1 or greater.

USE/ADVANTAGE - The sensor has a lower built-in strain and consequently is less affected by temperature related **drift** and operating range restrictions.

1/14

L10 ANSWER 3 OF 4 JAPIO COPYRIGHT 2002 JPO
AN 2001-203310 JAPIO
TI FLIP-**CHIP** IN MOLDING PACKAGE WITH LEADS AND MANUFACTURING METHOD THREFOR
IN JOSHI RAJEEV; TANGPUZ CONSUELO N; MANATAD ROMEL N
PA FAIRCHILD SEMICONDUCTOR CORP
PI JP 2001203310 A 20010727 Heisei
AI JP2000-381293 (JP2000381293 Heisei) 20001215
PRAI US 1999-464885 19991216
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
AB PROBLEM TO BE SOLVED: To provide a **chip** device having a **lead frame**, a **die** and a molding compound.
SOLUTION: When a back surface 14 of a **die** 12 is metallized and the **die** 12 is **coupled** to the **lead frame**, the **die** 12 is exposed via a **window** formed in an encapsulated mold compound 13. A lead 20 on the **lead frame** is **connected** to terminals of a source and a gate on the **die** 12. The metallized surface 14 of the **die** 12 functions as a **drain** terminal.
COPYRIGHT: (C)2001,JPO

L10 ANSWER 4 OF 4 JAPIO COPYRIGHT 2002 JPO
AN 1992-062943 JAPIO
TI SEMICONDUCTOR DEVICE
IN NAKAO YASUYOSHI
PA NEC CORP, JP (CO 000423)
PI JP 04062943 A 19920227 Heisei
AI JP1990-173051 (JP02173051 Heisei) 19900630
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1218, Vol. 16, No. 271, P. 15 (19920618)
AB PURPOSE: To inspect the disconnection state of a bonding wire electrically easily by a method wherein a plurality of semiconductor elements are divided and divided elements are **connected** respectively by using independent bonding wires.
CONSTITUTION: Unit cells are constituted in P-type diffusion layers arranged in an N-type silicon substrate 1. A gate oxide film 3 is formed on them. In addition, gates 4 are formed on it. N+ type source diffusion layers 5 are formed by making use of the gates 4 as masks. In addition, an interlayer insulating film 6 is grown; **windows** respectively corresponding to the gates 4 and the source diffusion layers 5 are **opened** and installed; a gate electrode 7 and a source electrode 8 are formed on the surface of the semiconductor substrate 1 including the **windows**. At this time, the source electrode 8 is divided into groups for the arbitrary number of unit cells; and it is formed independently at each group (a first source electrode 8A and a second source electrode 8B). A **drain** electrode 9 is formed on the rear face of the semiconductor substrate 1. A semiconductor **chip** C is **mounted** on an element-**mounting** part 12 of a **lead frame** 11; and the gate electrode 7 and a gate terminal G as well as the first and second source electrodes 8A, 8B and a source terminal S

are **connected** electrically by using bonding wires 13.

circuit devices are used in consumer electronics, computers, automobiles, telecommunications, and military applications. The system is also used in electroplating jewelry articles and electronic devices.

ADVANTAGE - A **drain** for water contaminated by drag out from the plating solution is eliminated. A significant cost savings is realized by avoiding a need for waste recovery associated with water for contact cooling. Use of the system reduces electroplating cost, while increasing plating productivity at reduced number of steps, process time, and chemical cost.

DESCRIPTION OF DRAWING(S) - The figure shows detail of 2 cells which include integrated solution cooling.

Cathode 100

Plating solution 111

Plating cells 410

Contact cell 420

Dwg.5a/7

L12 ANSWER 5 OF 16 WPIX (C) 2002 THOMSON DERWENT
AN 2000-097597 [08] WPIX
DNN N2000-075420 DNC C2000-028351
TI Package for semiconductor devices e.g. power metal oxide semiconductor field-effect transistors.
DC L03 U11
IN BAJE, G S; BENCUYA, I; ESTACIO, M C B; MALIGRO, R D; SNAPP, S P; TANGPUZ, C N
PA (FAIH) FAIRCHILD SEMICONDUCTOR CORP
CYC 22
PI WO 9965077 A1 19991216 (200008)* EN 15p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: CN JP KR
TW 423136 A 20010221 (200138)
ADT WO 9965077 A1 WO 1999-US12411 19990603; TW 423136 A TW 1999-109550 20000103
PRAI US 1998-141184 19980827; US 1998-88651P 19980609
AB WO 9965077 A UPAB: 20000215

NOVELTY - A package comprises a silicon **die** (202) encapsulated by a protective molding, solder **balls** (204) in contact with a conductive layer on a top surface of the **die** and a first metal **lead frame** (206) extending outside the protective molding.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a packaging method for a silicon **die** (202) comprising disposing the solder **balls** (204) on the top surface of the **die**, bringing the first **lead frame** (206) in direct contact with the **balls**, directly **attaching** the substrate side of the **die** to the second **lead frame** (200) using a **die attach** process and encapsulating the **die** with a protective mold such that the first and second **lead frames** extend outside the mold.

USE - The package is for semiconductor devices e.g. power MOSFETs.

ADVANTAGE - Allows the size and shape of the **lead frame** to be tailored to fit the device and to minimize its electrical and thermal resistance.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the wireless package.

drain lead frame 200

silicon **die** 202

solder **balls** 204

source top **lead frame** 206

gate top **lead frame** 208
Dwg.2/4

L12 ANSWER 6 OF 16 WPIX (C) 2002 THOMSON DERWENT
AN 1999-619764 [53] WPIX
DNN N1999-457053
TI **Chip**-on-**chip** modules interconnecting structure for **chip**-on-**chip** semiconductor package.
DC U11 U14
IN BERTIN, C L; FERENCE, T G; HOWELL, W J; SPROGIS, E J
PA (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP
CYC 5
PI US 5977640 A 19991102 (199953)* 12p
CN 1241032 A 20000112 (200022)
JP 2000156461 A 20000606 (200035) 10p
JP 3096459 B2 20001010 (200052) 10p
KR 2000005670 A 20000125 (200063)
TW 423082 A 20010221 (200138)
ADT US 5977640 A US 1998-105419 19980626; CN 1241032 A CN 1999-107091 19990527; JP 2000156461 A JP 1999-151409 19990531; JP 3096459 B2 JP 1999-151409 19990531; KR 2000005670 A KR 1999-17553 19990517; TW 423082 A TW 1999-107987 19990517
FDT JP 3096459 B2 Previous Publ. JP 2000156461
PRAI US 1998-105419 19980626
AB US 5977640 A UPAB: 19991215
NOVELTY - Solder **balls** (86) in a substrate (88) are arranged in a plane with the back side of one **chip** of each **chip**-on-**chip** module. Metallic pads (82) are arranged in a plane with the back side of another **chip** of each module to **connect** the **stacked** modules. The solder **balls** are **connected** to a **lead frame**.

DETAILED DESCRIPTION - Each module has two **chips** of different technologies, where **active regions** are electrically **connected**. The solder **balls** and metallic pads are **connected** to the **active regions** through conductive lines.

USE - For interconnecting a **chip**-on-**chip** module for a compact **chip**-on-**chip** semiconductor package.

ADVANTAGE - Offers very high level integration by using several dissimilar semiconductor devices. Improves component speed, bandwidth requirement and off-**chip** speed. Improves yield at low cost by using a **chip** formed by simple technology. Facilitates easy accommodation of **chips** of different sizes and thickness. Enables effective thermal management in inter unit structure size. Improves the electrical, mechanical, and thermal performance of a semiconductor package.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the **chip**-on-**chip** package.

Chip-on-**chip** component 80
Metallic pad 82
Solder **ball** 86
Substrate 88
Dwg.15/18

L12 ANSWER 7 OF 16 WPIX (C) 2002 THOMSON DERWENT
AN 1995-039298 [06] WPIX
DNN N1995-031144 DNC C1995-017428
TI Packaging power semiconductor device to improve high frequency characteristics - by providing **lead frame** with paddle,

on which semiconductor **chip** is located, with Kovar (RTM) **plate** having similar thermal expansion coefft. to **chip**, etc..

DC A85 U11

IN KANG, S; KIM, D; PARK, H; PARK, S; SONG, M; YOON, H; PARK, H M; KIM, S; YUN, H

PA (ELTE-N) ELECTRONICS & TELECOM RES INST; (KANK-N) ZH KANKOKU DENSHI TSUSHIN KENKYUSHO; (KOEL-N) KOREA ELECTRONICS & TELECOM RES; (KOTE-N) KOREA TELECOM CORP

CYC 6

PI	GB 2280062	A	19950118 (199506)*	18p
	DE 4424549	A1	19950119 (199508)	8p
	FR 2707798	A1	19950120 (199509)	
	JP 07078900	A	19950320 (199520)	6p
	US 5446959	A	19950905 (199541)	7p
	DE 4424549	C2	19961017 (199646)	8p
	US 5612853	A	19970318 (199717)	7p
	GB 2280062	B	19970409 (199718)	
	KR 9600706	B1	19960111 (199906)	

ADT GB 2280062 A GB 1994-13867 19940708; DE 4424549 A1 DE 1994-4424549 19940712; FR 2707798 A1 FR 1994-8824 19940711; JP 07078900 A JP 1994-159894 19940712; US 5446959 A US 1994-268104 19940706; DE 4424549 C2 DE 1994-4424549 19940712; US 5612853 A Div ex US 1994-268104 19940706, US 1995-381304 19950131; GB 2280062 B GB 1994-13867 19940708; KR 9600706 B1 KR 1993-13085 19930712

FDT US 5612853 A Div ex US 5446959

PRAI KR 1993-13085 19930712

AB GB 2280062 A UPAB: 19950404

Package for power semiconductor device has **lead frame** (10) including a body (11), a paddle (12) on which the power semiconductor **chip** (40) is located, tie bars (15,16) **connecting** body and paddle and supporting opposite sides of the paddle, and gate and **drain** electrode leads (13,14) **connected** to opposite sides of the body respectively. A heat radiating **plate** (20) is **attached** to the bottom surface of the paddle and a Kovar (RTM) **plate** (30), having similar thermal expansion coefft. to that of the semiconductor **chip**, is formed on the paddle. A polyimide layer having predetermined thickness is formed over the semiconductor **chip**, a metal cap (50) is fitted over the paddle and electrically **connected** to the tie bars by soldering, and an epoxy resin layer is moulded over the metal cap. The **chip** is electrically **connected** to the Kovar **plate** by soldering and respective terminals of the **chip** are electrically **connected** to leads of the **lead frame** by wire bonding. The paddle is provided at a lower horizontal level than the gate electrode lead.

Pref. the tie bars are impedance-matched to a source electrode lead of the **lead frame**, the source electrode of the semiconductor **chip** being grounded through the tie bars to serve as the source electrode lead.

ADVANTAGE - The semiconductor device has improved high frequency characteristics and the packaging is suitable for mass prodn. by low mfg. cost.

Dwg.2A,2C/2

L12 ANSWER 8 OF 16 WPIX (C) 2002 THOMSON DERWENT

AN 1994-203951 [25] WPIX

DNN N1994-160627

TI **Chip** carrier - has external lead for gate and external lead for **drain connected** to metal frame base **plate**

through **frame** and external **lead** for source, so electric conductivity is kept among above leads and base **plate**
NoAbstract.
DC U11
PA (MITQ) MITSUBISHI ELECTRIC CORP
CYC 1
PI JP 06140530 A 19940520 (199425)* 5p
ADT JP 06140530 A JP 1992-316199 19921028
PRAI JP 1992-316199 19921028
AB JP 06140530 A UPAB: 19940810
Dwg.1/1

L12 ANSWER 9 OF 16 WPIX (C) 2002 THOMSON DERWENT
AN 1980-K1982C [42] WPIX
TI **Connector** assembly with **lead frame** **mounting** for semiconductor **chips** - has optically **active areas**, fibre guide and optical fibres held in communication with **chips**.
DC P81 U11 U12 V07
IN DELAGI, R G; MCBRIDE, L E
PA (TEXI) TEXAS INSTR INC
CYC 1
PI US 4225213 A 19800930 (198042)*
PRAI US 1977-863758 19771223
AB US 4225213 A UPAB: 19930902
The fibre guide is formed of a **plate** like member having two or more reference points, in order to precisely locate fibres relative to the **chip**. Several embodiments of the guide are available including a **plate** having fibre receiving bores extending through as well as a **plate** having fibre receiving grooves extending along sides thereof pref. used in conjunction with a bar biased against fibres disposed in the grooves.

The bar, which may be made of elastomeric material is shown having a straight edge facing the grooves while a variation of the bar is provided with an additional set of grooves. The **lead frame** **mounts** a relatively large thermally and electrically conductive pad which in turn **mounts** the semiconductor **chip** having optically **active area**. Fibres are trained through respective bores or grooves and epoxied in alignment with respective optically **active areas**.

L12 ANSWER 10 OF 16 WPIX (C) 2002 THOMSON DERWENT
AN 1980-A9317C [04] WPIX
TI **Connector** for interfacing electronic circuits and optical fibres - has housing **mounting** contact and semiconductor **chips** having optically **active areas**.
DC V05
IN MCBRIDE, L E
PA (TEXI) TEXAS INSTR INC
CYC 1
PI US 4184070 A 19800115 (198004)*
PRAI US 1977-863777 19771223
AB US 4184070 A UPAB: 19940205
The **connector** comprises a **lead frame** **mounting** semiconductor **chips**, a fibre guide and optical fibres held in optical communication with the **chips**. The fibre guide is formed of a **plate**-like member having two or more reference points to precisely locate the fibres relative to the **chip**.

A **plate** has fibre-receiving bores as well as a **plate** having fibre-receiving grooves extending along the sides. The **lead frame mounts** a thermal and electrically conductive pad which **mounts** the semiconductor **chip** having optically **active areas**. The **connector** is adapted to be **mounted** on one side of a backplane while the electronic components such as drivers and amplifiers are **mounted** on a second side of the back plane.

L12 ANSWER 11 OF 16 JAPIO COPYRIGHT 2002 JPO
AN 2001-351941 JAPIO
TI FLIP-CLIP **ATTACH** AND COPPER CLIP **ATTACH** ON MOSFET DEVICE
IN ESTACIO MARIA CHRISTINA B; KUINONESU MARIA CLEMENS Y
PA FAIRCHILD SEMICONDUCTOR CORP
PI JP 2001351941 A 20011221 Heisei
AI JP2001-114665 (JP2001114665 Heisei) 20010412
PRAI US 2000-548946 20000413
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
AB PROBLEM TO BE SOLVED: To provide a method of manufacturing a **chip** which includes direct **mounted** the **chip** devices and **dies** with **bumps** on a **lead frame** and the **attachment** of a set of leads to the **dies** with **bumps**, using clips.
SOLUTION: The method of manufacturing a **chip** includes a step of providing the **dies** with **bumps** having a plurality of solder humps, a step of providing the **lead frame** having source and gate **connections**, and a step arranging the **dies** with **bumps** on the **lead frame**, so that the solder **bumps** come into contact with the source and gate **connections**. The method also includes a step of **attaching** copper clips to the rear surfaces of the **dies** with **bumps** using solder paste, so that the clips come into contact with the **drain** regions and lead rails of the **dies** with **bumps** and a step of reflowing the solder paste and solder **bumps**.
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L12 ANSWER 12 OF 16 JAPIO COPYRIGHT 2002 JPO
AN 2000-077588 JAPIO
TI HIGH CURRENT CAPACITY SEMICONDUCTOR DEVICE PACKAGE AND **LEAD FRAME** WITH LARGE AREA **CONNECTION** POST AND MODIFIED OUTLINE
IN WOODWORTH ARTHUR; EWER PETER R; TEASDALE KEN
PA INTERNATL RECTIFIER CORP
PI JP 2000077588 A 20000314 Heisei
AI JP1999-161451 (JP11161451 Heisei) 19990430
PRAI US 1998-84224 19980505
US 1998-103035 19980623
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To obtain a high current capacity semiconductor device package and **lead frame** with large area **connection posts** and modified outline.
SOLUTION: This **lead frame** of a high power semiconductor device **die** has three outer lead conductors 25, 26, 27 which can be gate, **drain** and source contacts of the **die**, respectively. Two outer lead conductors are bent to recede from the center of the lead 26 and a package 20 by means of recessed bends 30, 31. Since the creeping distances 32, 33 along a face 28 is increased,

a higher voltage can be applied between the leads 25, 27 and the central lead 26.

L12 ANSWER 13 OF 16 JAPIO COPYRIGHT 2002 JPO
AN 1992-284659 JAPIO
TI SEMICONDUCTOR DEVICE
IN SATO KENGO
PA TOSHIBA CORP, JP (CO 000307)
PI JP 04284659 A 19921009 Heisei
AI JP1991-48408 (JP03048408 Heisei) 19910313
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1324, Vol. 17, No. 91, P. 40 (19930223)
AB PURPOSE: To manufacture the title compact and highly reliable semiconductor device by a method wherein at least a part of the surface of a semiconductor **chip** is covered with an insulating film; a bonding pad is re-wired to the surface of the insulating film; and then an inner lead is **connected** to the bonding pad by direct junctioning step.
CONSTITUTION: At least one bonding pad 10 is re-wired to an element region of a semiconductor **chip** 1 through the intermediary of an insulating layer 7 while the inner leads 2 of a **lead frame** extending over said bonding pad 10 are **connected** by direct junctioning step. For example, the whole surface containing the **active** element **region** of the semiconductor **chip** 1 is covered with the polyimide resin film 7 while the re-arrayed wiring 11 containing the re-arrayed electrode 10 is re-arrayed on the **active** element **region** so that the polyimide resin film 7 may be **connected** to the other bonding pad 12 via through hole h made in the polyimide film 7. On the other hand, the ends of the inner leads 2 are directly junctioned with the re-arrayed electrode 10 by a **bump** 6 while the outer side is coated with a sealing resin 9.

L12 ANSWER 14 OF 16 JAPIO COPYRIGHT 2002 JPO
AN 1991-109748 JAPIO
TI SEMICONDUCTOR DEVICE
IN SERIZAWA KOJI; SAKAGUCHI MASARU; KANEDA AIZO
PA HITACHI LTD, JP (CO 000510)
PI JP 03109748 A 19910509 Heisei
AI JP1989-246488 (JP01246488 Heisei) 19890925
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1096, Vol. 15, No. 3, P. 152 (19910805)
AB PURPOSE: To achieve an ultra multi-pin configuration and low noise by configuring so that an electrode is pulled out of the whole surface of a semiconductor **chip** and by **connecting** a substrate of each layer of the multilayer substrate and a **lead frame** separately.
CONSTITUTION: The title item has a semiconductor **chip** 7, a multilayer substrate 9, a **lead frame** 10, and first and second mold resins 17 and 18. Then, a BPA for forming a **bump** 8 by multilayer wiring on an **active** element **region** on the **chip** 7 is adopted so that an electrode can be pulled out of the entire surface of the **chip** 7. The **lead frame** 10 is sandwiched at the peripheral part of the substrate 9, a substrate surface electrode 12 is provided at a position corresponding to the **bump** 8 of the **chip** 7 in the substrate of each layer of the substrate 9, and the electrode **plate** 12 of each layer and the **lead frame** 10 are **connected** with a solder plating 16 which is executed in a through-hole 15 which is

provided between the layers of the substrate 9, thus achieving an ultra multi-pin configuration and low noise.

L12 ANSWER 15 OF 16 JAPIO COPYRIGHT 2002 JPO
AN 1984-047752 JAPIO
TI SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF
IN MARUYAMA YASUO; KANBAYASHI KAZUO
PA HITACHI LTD, JP (CO 000510)
PI JP 59047752 A 19840317 Showa
AI JP1982-156645 (JP57156645 Showa) 19820910
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 253, Vol. 8, No. 1391, P. 14 (19840628)
AB PURPOSE: To stabilize a lead inductance and increase an electrostatic destruction strength by securing a second **chip** in a recess part formed by etching at the region being apart from the second element forming region of supported **chip** region and securing **wafers** dividingly for each supported **chip** region.
CONSTITUTION: A P type conductive region 13 is formed at a part of the main surface layer of a square supported **chip** region 21, a recess 17 which engages with a GaAs **chip** 3 is provided, by the anisotropic etching, to the main surface at the outside of the protection diode region by the p-n junction 14, and the GaAs **chip** 3 absorbed and held in vacuum condition by the collet 23 is secured through the Ag paste 18. A supported **chip** is divided for each supported **chip** region into supported **chips** 12. Thereafter, these **chips** are absorbed and held in vacuum condition by the collet 24 and are secured on the **chip** loading **plate** 8 of **lead frame** consisting of the source lead 7, gate lead 10 and **drain** lead 11 through the silver paste 16. Next, the supported **chip** 12, electrode of GaAs 3, internal end of lead 2 corresponding thereto and electrodes are **connected** by wires.

L12 ANSWER 16 OF 16 JAPIO COPYRIGHT 2002 JPO
AN 1981-164561 JAPIO
TI SEMICONDUCTOR DEVICE
IN NISHI KUNIHIKO; WAKASHIMA YOSHIAKI
PA HITACHI LTD, JP (CO 000510)
PI JP 56164561 A 19811217 Showa
AI JP1980-67808 (JP55067808 Showa) 19800523
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 100, Vol. 6, No. 521, P. 15 (19820407)
AB PURPOSE: To provide a device with a better protection against humidity, by covering the device, which is held in a cavity-type package of a resin-formed body, with a defective-free passivation film such as a nitride film and also by covering an electrode with an Au **bump**.
CONSTITUTION: An **IC chip** 2 is **joined** to a tab 1a of a **lead frame**, and a **lead** 1b is tightly caught between top and bottom cavity-type packages 3 and 4. A passivation film 8 which is to protect an **active region** of this **IC chip** 2 is used by being provided with a defect-free film such as an SiO2 film formed on a PSG film by a nitride film, a polyimide-type resin film or a spatter. And an Au **bump** electrode 9 is **connected** through a through hole of the passivation film 8 to an Au electrode 7 provided on the **chip** 2, and it is bonded to the lead 1b by an Au wire 10. It is possible, by doing so, to provide a humidity-proof and highly reliable resin package, and by employing cavity type, it becomes possible to easily automate the operation and also to **mount** a large-size **chip**.

D BIB AB 1-21

L14 ANSWER 1 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 2001-637691 [73] WPIX
DNN N2001-476525
TI Semiconductor device package in which heat generated in MOSFET **die** is conducted to main pad area of **lead frame** and then to pins extending out from **lead frame**.
DC U11
IN CHEAH, C; KINZER, D M; MUNOS, J
PA (INRC) INT RECTIFIER CORP
CYC 1
PI US 6242800 B1 20010605 (200173)* 6p
ADT US 6242800 B1 US 1997-815814 19970312
PRAI US 1997-815814 19970312
AB US 6242800 B UPAB: 20011211
NOVELTY - A MOSFET **die** (10) is **mounted** over main pad area (41) of **lead frame** (40) comprising a set of pins (1-6) extending symmetrically from two side edges of frame. The **die** and **lead frame** are enclosed within molded housing (30). The heat generated by MOSFET is conducted to main pad area and then to pin which are bent along side edges of housing. Then, the heat is conducted to external substrate.
DETAILED DESCRIPTION - The **drain** electrode of MOSFET contacts bottom surface of main pad area and is electrically **connected** to pins. The source electrode (10B) and **gate** electrode (10C) are formed over main surface of pad area and **connected** to pins. The height of molded housing ranges from 0.9-1.45 mm.
USE - Semiconductor device package with heat dissipation function.
ADVANTAGE - Enables efficient removal of heat from package and reduces height of package.
DESCRIPTION OF DRAWING(S) - The figure shows the sectional bottom view of semiconductor package.
Pins 1-6
MOSFET **die** 10
Source electrode 10B
Molded housing 30
Lead frame 40
Main pad area 41
Dwg.3/5

L14 ANSWER 2 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 1998-373263 [32] WPIX
DNN N1998-292908
TI Structure of semiconductor device used in high frequency wireless communication - has bonding wire to **connect** spiral lead terminal, first and second lead terminal to **gate** electrode, source and **drain** electrodes respectively.
DC U11 V02
PA (NIDE) NEC CORP
CYC 1
PI JP 10150068 A 19980602 (199832)* 4p
JP 3130809 B2 20010131 (200109) 4p
ADT JP 10150068 A JP 1996-308486 19961119; JP 3130809 B2 JP 1996-308486 19961119
FDT JP 3130809 B2 Previous Publ. JP 10150068
PRAI JP 1996-308486 19961119
AB JP 10150068 A UPAB: 19980812

The structure includes a **lead frame** with a spiral lead terminal (101). An edge portion (101a) is formed in the lead terminal. A **chip mounting** area (105) with a GaAsFET (104) is formed in the lead terminal. A first lead terminal (102) is drawn out from the **chip mounting** area.

A second lead terminal (103) is provided adjacent to the **chip mounting** area. A **gate**, **drain** and source electrodes (107,108,109) are **connected** to the spiral lead terminal, second and first lead terminal respectively, by a bonding wire (106). An epoxy resin (110) seals the **connected** terminals.

ADVANTAGE - Obtains favourable characteristic. Reduces reflex of input-output signal.

Dwg.1/4

L14 ANSWER 3 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 1998-361897 [31] WPIX
DNN N1998-282549
TI Power MOSFET layout - includes **gate**-runners dividing **source** contact **area** into sub-contact areas which have different sizes, giving uniformly distributed lead-wire contact points.
DC U11 U12
IN HU, Y; MA, T
PA (MAGE-N) MAGEMOS CORP
CYC 1
PI US 5767567 A 19980616 (199831)* 12p
ADT US 5767567 A US 1996-707929 19960910
PRAI US 1996-707929 19960910
AB US 5767567 A UPAB: 19980805

The layout includes a MOSFET power **integrated circuit** device (100) disposed in a semiconductor **chip**, **mounted** on a **die** pad (110) and surrounded by **lead frames** (120). The device includes a **source** contact **area** (150).

A number of **gate**-runners (140) are on the **source** contact **area**, dividing it into several sub-contact areas (150-1 to 150-4) which are arranged with different sizes for giving uniformly distributed lead-wire contact points (170). Lead-wires (160) are secured to the contact points and **connect** to the **lead frames**.

ADVANTAGE - The uniformly distributed contact points result in a reduced spread resistance whereby the device on-resistance and performance may be improved.

Dwg.2B/5

L14 ANSWER 4 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 1997-502439 [46] WPIX
DNN N1997-418826
TI No-bond **integrated circuit** inputs for **integrated circuit die** - selectively bonds to supply **lead-frame** finger and supply logic to pull unconnected input to proper voltage.
DC U11
IN LINDLEY, D R
PA (CYPR-N) CYPRESS SEMICONDUCTOR CORP
CYC 1
PI US 5675178 A 19971007 (199746)* 6p
ADT US 5675178 A US 1995-561948 19951122
PRAI US 1995-561948 19951122
AB US 5675178 A UPAB: 19971119

The **integrated circuit** (**IC**) has a supply pad, a no-**connect** (NC) input pad, and an **IC** input pad, in combination with **IC** logic and an input **leadframe** finger (14) and a supply voltage **leadframe** finger (13), which is **connected** to one of two supply voltages of opposite polarity, and the supply pad. The **IC** input pad is to be no-bonded. The **connections** comprise the NC input pad is **coupled** to the common **connection**, between the **drain** of a leaker transistor (15) and the **gate** of a strong transistor (16) in the **IC** logic.

The leaker and strong transistors have their sources **coupled** to the other of the two voltages of opposite polarity from the one supply voltage **coupled** to the supply voltage **leadframe** finger. The **IC** input pad is **coupled** to the **drain** of strong transistor. A bond wire **couples** NC input pad to supply voltage **leadframe** finger, for pulling **IC** input pad to the other of two supply voltages, from supply voltage **connected** to supply voltage **leadframe** finger.

USE/ADVANTAGE - Selectively **connects** no-bond **IC** input to supply rail of proper polarity. Can overcome problems with noisy input voltages.

Dwg.1/3

L14 ANSWER 5 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 1997-361268 [33] WPIX
DNN N1997-300325
TI **Lead frame** structure for HF usage type semiconductor device e.g. FET, HEMT - has second pair of lead pieces, whose input and output terminals are **connected** to **gate** and **drain** electrodes of semiconductor **chip mounted** onto bed part, respectively.
DC U11
PA (TOKE) TOSHIBA KK
CYC 1
PI JP 09153577 A 19970610 (199733)* 5p
ADT JP 09153577 A JP 1995-312113 19951130
PRAI JP 1995-312113 19951130
AB JP 09153577 A UPAB: 19970813

The structure (11) sealed by a resin material, comprises a rectangular bed part (14), on middle of which, a semiconductor **chip** (17) is **mounted**. A first pair of lead piece wires (12,13) is formed at both ends of the bed part, respectively. A second pair of lead pieces (15,16) is formed between sides of the bed part. The source electrode of the semiconductor **chip** is **connected** to the bed part.

The **gate** and **drain** electrodes of the semiconductor **chip** are **connected** to the respective signal input-output terminal of the second piece of lead pieces through bonding wires. The first pair of lead pieces act as grounding conductor.

ADVANTAGE - Reduces cost by using cheap resin material as envelope. Assures heat dissipation characteristics. Facilitates operation of semiconductor device, irrespective of structure of semiconductor **chip mounted** onto bed part.

Dwg.1/3

L14 ANSWER 6 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 1994-287497 [36] WPIX
DNN N1994-226407
TI Buffer with pull-up and pull-down circuitry esp. output buffer in programmable array **logic circuit** - has pull-down

transistor, **connected** to noisy ground, switched on e.g. by one-shot pulse, in response to pull-down turn-on signal, and then switched off as pull-down transistor, **connected** to quiet ground, is switched on by delay signal.

DC U11 U13 U21
IN SHARPE-GIESLER, B A; SHARPE-GEISLER, B A
PA (ADMI) ADVANCED MICRO DEVICES INC
CYC 15
PI EP 616430 A2 19940921 (199436)* EN 19p
R: BE DE DK ES FR GB GR IE IT LU NL PT SE
JP 07050573 A 19950221 (199517) 15p
US 5438277 A 19950801 (199536)
US 5570046 A 19961029 (199649) 15p
US 5583451 A 19961210 (199704) 15p
EP 616430 A3 19970604 (199732)
ADT EP 616430 A2 EP 1994-301383 19940225; JP 07050573 A JP 1994-36924 19940308; US 5438277 A US 1993-34549 19930319; US 5570046 A Div ex US 1993-34549 19930319, US 1995-453184 19950530; US 5583451 A Div ex US 1993-34549 19930319, US 1995-453479 19950530; EP 616430 A3 EP 1994-301383 19940225
FDT US 5570046 A Div ex US 5438277; US 5583451 A Div ex US 5438277
PRAI US 1993-34549 19930319; US 1995-453184 19950530; US 1995-453479 19950530
AB EP 616430 A UPAB: 19941102
The buffer includes two pull-down transistors, a noisy transistor and a quiet transistor. A switching circuit turns on the noisy transistor in response to a pull-down circuit turn-on signal. The switching circuit responds to a time delay signal to turn on the quiet transistor and to turn off the noisy transistor, where the time delay signal is generated after a set time interval in response to the pull-down circuit turn-on signal. The buffer may include a quiet lead and a noisy lead, **connected** respectively to the quiet and noisy transistors, and both overlying a floating conductive plane.

The leads may **connect** the corresp. transistors to noisy and quiet ground terminals, where the transistors are identified as noisy or quiet due to their **connection** to the corresp. ground terminal. The buffer output is held low by the quiet transistor. The pull-up circuitry pref. operates ina similar way. The quiet and noisy ground leads may be **connected** to a single **lead frame** pin.

ADVANTAGE - Limits ground bounce, without limiting output slew rate; limits lead self and mutual inductance; increased operating speed.
Dwg.3/12

L14 ANSWER 7 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 1993-291770 [37] WPIX
DNN N1993-224679
TI Cutting machine for lead terminal in photo interrupter - **couples** and loads **lead frame** with interrupters by transferring it to **die** metallic mould, reciprocates punch header, and cuts lead terminal without leaving waste in punch hole NoAbstract.
DC U11 U12
PA (ROHL) ROHM CO LTD
CYC 1
PI JP 05206511 A 19930813 (199337)* 8p
JP 3016937 B2 20000306 (200016) 8p
ADT JP 05206511 A JP 1992-14233 19920129; JP 3016937 B2 JP 1992-14233 19920129
FDT JP 3016937 B2 Previous Publ. JP 05206511
PRAI JP 1992-14233 19920129

L14 ANSWER 8 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 1989-122327 [16] WPIX
DNN N1989-093347
TI MOSFET based direct current sensor lead - has jumper wire **connected** to MOSFET source pad and permits direct **gate** return referencing.
DC U11 U12
PA (KAUF-I) KAUFMAN L R
CYC 1
PI US 4818895 A 19890404 (198916)* 8p
ADT US 4818895 A US 1987-120632 19871113
PRAI US 1987-120632 19871113
AB US 4818895 A UPAB: 19930923
The direct current sense load includes a semiconductor **chip** such as a MOSFET (12) **mounted** on a **drain** terminal **lead frame** (6) on a ceramic substrate (4). A combined source and **gate** return reference jumper wire (40) is **connected** between a current sense **lead frame** (52) and a combined **gate** return reference and current sense **lead frame** (38). the jumper wire has a middle portion (42) **connected** to the source pad (14) of the MOSFET **chip** , and has another **connected** to the source terminal **lead frame** (8). Direct **gate** return referencing is provided, minimizing inductance in the **gate** return which is otherwise present when the **gate** return current path shares a portion of the source terminal current path.

Direct current sensing is also provided, and the IR drop is sensed across the section of the wire jumper between the middle portions (42 and 58), without the need of an auxiliary resistor in series with the source terminal. A gold wire (62) is bonded to an aluminium jumper wire (40) directly at the MOSFET source pad to provide a thermocouple for direct junction temperature sensing.

ADVANTAGE - Enhanced current density accuracy.

2/6

L14 ANSWER 9 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 2000-082816 JAPIO
TI LOW-POWER **MOUNTING** DESIGN
IN HEWITT CHARLES
PA HARRIS CORP
PI JP 2000082816 A 20000321 Heisei
AI JP1999-221075 (JP11221075 Heisei) 19990804
PRAI US 1998-129321 19980805
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To provide a semiconductor device that is lessened in power consumption by a method wherein a **source region** and a channel region are provided on a first plane, and a **drain** region is formed on a second plane to provide a **drain** contact. SOLUTION: A semiconductor device is **attached** to a **connector**, and the **connector** is held on a **lead frame**. The **lead frame** is moved to a **die mounting** station where a power MOSFET is mechanically and electrically **connected** to the **connector** . The MOSFET is equipped with a first plane possessed of an N+ **source region** 93, a P-type bulk region 94, and a **drain** region 95. The **drain** region 95 is extended to the power MOSFET, a **drain** contact metal layer 96 on a second plane is brought into low ohmic contact with the **drain** region 95. An insulating layer 91 and a conductive **gate** 92 are formed on a

cannel region 98, and a MOSFET 90 is equipped with a **drain** contact 96. By this setup, a semiconductor device of this constitution can be lessened in power loss caused by the resistance of a **connector** .

L14 ANSWER 10 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1999-150272 JAPIO
TI SEMICONDUCTOR SWITCHING ELEMENT
IN SUZUMURA MASAHIKO; YOSHIDA TAKESHI; TAKANO MASAMICHI; KISHIDA TAKASHI; SHIRAI YOSHIFUMI; HAYAZAKI YOSHIKI; SUZUKI YUJI
PA MATSUSHITA ELECTRIC WORKS LTD, JP (CO 000583)
PI JP 11150272 A 19990602 Heisei
AI JP1997-314029 (JP09314029 Heisei) 19971114
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 99, No. 6
AB PURPOSE: TO BE SOLVED:To provide a semiconductor switching element, wherein the back side of a semiconductor support substrate is **mounted** on a conductive substrate, and when one of a pair of output electrodes is electrically **connected** to the conductive substrate, the output capacitance between the output electrodes can be reduced.
CONSTITUTION: switch element comprises an n-type semiconductor layer 1 formed on an n-type Si-made semiconductor support substrate 10 via an insulation layer 11 with a **drain** electrode 7, a source electrode 8 and a **gate** electrode 6b formed on the surface of the semiconductor layer 1, and an insulation film 12 on the back side of the support substrate 10. The support substrate 10 is **die**-bonded to the conductive substrate, composed of a **lead frame** to electrically **connect** the source electrode 8 to the conductive substrate. The capacitance between the **drain** electrode 7 and the conductive substrate is a series of a first parasitic capacitance component which is formed between the semiconductor layer 1 and support substrate 10 and a second parasitic capacitance component resulting from the insulation film 12.

L14 ANSWER 11 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1999-126867 JAPIO
TI SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF
IN SATO TAKU
PA NEC CORP, JP (CO 000423)
PI JP 11126867 A 19990511 Heisei
AI JP1997-291114 (JP09291114 Heisei) 19971023
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 99, No. 5
AB PURPOSE: TO BE SOLVED:To inhibit the deterioration of the characteristics of a semiconductor device due to parasitic capacitance or the like and to contrive to improve the reliability of the device by a method wherein a sealed space encircled with microscopic walls formed to encircle an operating region on a semiconductor substrate, excepting pad electrodes, to consist of a conductor and a **lead frame**, is formed.
CONSTITUTION: ce ohmic electrodes 6, a **drain** ohmic electrode 5, and **gate** electrodes 7 are arranged on a semiconductor substrate 2 in the horizontal direction of the substrate 2. Moreover, source pad electrodes (microscopic walls) 13, a **drain** pad electrode 11 and a **gate** pad electrode 12 are provided on an insulating film 15 on the substrate 2. Then, the electrodes 6, the electrode 5 and the electrodes 7 are all **connected** with electrodes 13, the electrode 11 and the electrode 12 via through-holes 14. The substrate 2 is subjected

to flip-**chip mounting** on a **lead** **frame** 1, whereby a sealed space 18 encircled with the electrodes 13 and the **lead frame** 1 is formed.

L14 ANSWER 12 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1998-247701 JAPIO
TI SEMICONDUCTOR DEVICE AND **LEAD FRAME** FOR MANUFACTURING THE SAME
IN TAKESHIMA HIDEHIRO; OOKA KANJI
PA HITACHI LTD, JP (CO 000510)
AKITA DENSHI KK, JP (CO 486002)
JAPAN ENERGY CORP, JP (CO 330259)
PI JP 10247701 A 19980914 Heisei
AI JP1997-50677 (JP09050677 Heisei) 19970305
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 98, No. 9
AB PURPOSE: TO BE SOLVED:To increase the **connection** strength and reliability of the wire **connecting** to a supporting board, by a method wherein an intrusion stopping means preventing a junction material from intruding into wire **connecting** regions is provided between a semiconductor fixing region and wire **connecting** regions. CONSTITUTION: rtial dent 10 is provided on the upper side of a supporting board 4 so as to fix a semiconductor **chip** 6 on the bottom face of the dent 10 through the intermediary of a junction material 5. The area of the dent 10 is made wider than that of a semiconductor **chip** fixing region 11 as shown by two point chain line. Besides, the dent 10 is formed toward the **drain** lead side so as to make the upper side part of the supporting board side toward the **gate** lead to be the edge part wider than the **drain** lead side for constituting a wire **connecting** part 12. Furthermore, the parts of the wire **connecting** part 12 are formed into wire **connecting** regions 13 as shown by two point chain lines. Accordingly, the upper sides of the wire **connecting** regions 13 are made higher than that of the semiconductor **chip** fixing region 11, thereby preventing the junction material 5 from creeping up the upper sides of the wire **connecting** regions 13.

L14 ANSWER 13 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1998-150068 JAPIO
TI SEMICONDUCTOR DEVICE
IN SATO TAKU
PA NEC CORP, JP (CO 000423)
PI JP 10150068 A 19980602 Heisei
AI JP1996-308486 (JP08308486 Heisei) 19961119
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 98, No. 6
AB PURPOSE: TO BE SOLVED:To provide a semiconductor device of a PKG (3-pin, small minimold package) structure which can be manufactured inexpensively and easily with low costs and with a sufficient inductance and excellent low noise characteristics. CONSTITUTION: As FET 104 is **mounted** on a **chip** **mount** area 105 of a **lead frame** having a **lead** terminal 101 with an end 101a of a spiral coil shape. The lead terminals 101, 102 and 103 are **connected** to **gate**, **drain** and source electrodes 107, 108 and 109 respectively, and the sealed with epoxy resin 110.

L14 ANSWER 14 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1994-061382 JAPIO

TI SEMICONDUCTOR COOLING DEVICE
IN WATARI SHIGERU
PA MATSUSHITA ELECTRIC IND CO LTD, JP (CO 000582)
PI JP 06061382 A 19940304 Heisei
AI JP1992-214877 (JP04214877 Heisei) 19920812
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1558, Vol. 18, No. 299, P. 54 (19940608)
AB PURPOSE: To enable heat released inside a MOSLSI to be dissipated outside the package to restrain it from raising temperature by a method wherein a groove of a depth larger than the diffusion depth of impurity in an **active region** is provided in the **active region**.
CONSTITUTION: In a MOSLSI, a groove 10 of a depth larger than the diffusion depth of impurity in an **active region** is provided in the **active region**. A metal thin film 12 is deposited covering the groove 10 and **connected** to a bonding pad 13 through a via-hole 7. The bonding pad 13 is **connected** to the inner terminal of a semiconductor package **lead frame** or a **die attaching** part 16 with a metal wire 14. By this setup, heat released from a transistor in operation can be quickly conducted from the upper part of a board to the **die attaching** part 16 of a package. Therefore, a heat transfer route from a heat releasing part to a **mounting** interface between a **chip** and a package can be lessened in thermal resistance.

L14 ANSWER 15 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1993-251632 JAPIO
TI SEMICONDUCTOR DEVICE
IN FUJISAWA NAOTO
PA FUJI ELECTRIC CO LTD, JP (CO 000523)
PI JP 05251632 A 19930928 Heisei
AI JP1992-47373 (JP04047373 Heisei) 19920305
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1486, Vol. 18, No. 8, P. 107 (19940107)
AB PURPOSE: To reduce by half the **mounting** area, by installing two semiconductor devices on one metal substrate.
CONSTITUTION: A P channel MOSFET **chip** 11 is installed on one face of a **mounting** part 2 of a **lead frame** acting as a heat dissipation substrate by a **die** bonding. Similarly, an N channel MOSFET **chip** 12 is fixed on the other face of the **mounting** part 2. By **connecting** **drain** electrodes of both the **chips** 11 and 12 to the **mounting** part 2, both the MOSFET **chips** 11 and 12 are **connected** in series. A source pad 3 of both the **chips** 11 and 12 is **connected** to external lead parts 51 and 53 by a bonding of an Al wire 6. A **gate** pad 4 is **connected** to an external lead part 52 by the bonding of the Al wire 6 on both faces. By securing semiconductor devices on both faces of the heat dissipation substrate, the **mounting** area with a complementary construction can be reduced by half.

L14 ANSWER 16 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1992-137753 JAPIO
TI HIGH FREQUENCY SEMICONDUCTOR DEVICE
IN ANDO MAMORU; AZUMI TOSHIAKI
PA SANYO ELECTRIC CO LTD, JP (CO 000188)
PI JP 04137753 A 19920512 Heisei
AI JP1990-262494 (JP02262494 Heisei) 19900928
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No.

1255, Vol. 16, No. 4, P. 163 (19920828)
AB PURPOSE: To improve high frequency characteristics by potting the periphery of a GaAs semiconductor **chip** with a first resin composed of polyimide resin having low permittivity and then molding the main part with a second resin having high permittivity.
CONSTITUTION: A GaAs semiconductor **chip** 11 is bonded through an adhesive 19 onto an island 12 of a **lead frame**.
Electrode pads, corresponding to the **gate**.cntdot.source and the **drain**, are formed on the surface of the GaAs semiconductor **chip** 11 and wire bonded with external **connection** leads 13, 14, 15 through a gold wire 16. The GaAs semiconductor **chip** 11 on the island 12 is then potted with a first resin 17 while wrapping the gold wire 16, the resin is cured, and then the **chip** 11 is molded with a second resin 18 by transfer molding. Polyimide resin is employed as the first resin and a thermosetting epoxy resin is employed as the second resin 18. According to the constitution, stray capacity between the **gate** and the **drain** can be reduced and even a mold type device can be manufactured without sacrifice of high frequency characteristics.

L14 ANSWER 17 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1991-265149 JAPIO
TI SEMICONDUCTOR DEVICE
IN OTA MASAKI
PA TOSHIBA CORP, JP (CO 000307)
PI JP 03265149 A 19911126 Heisei
AI JP1990-62789 (JP02062789 Heisei) 19900315
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1170, Vol. 16, No. 74, P. 12 (19920224)
AB PURPOSE: To make possible the **connection** of a thick wire to a pad for power leadout use and to enable a semiconductor device to fulfill sufficiently its electrical characteristics by a method wherein one **chip** is **connected** with the outside using bonding wires composed of different materials.
CONSTITUTION: When a semiconductor **chip** 12 **mounted** on a **die** pad 11 of a **lead frame** is constituted of a signal processing part 12a comprising a bipolar transistor and a CMOSFET and a power part 12b comprising a power MOSFET, the **connection** of these parts with inner leads is conducted as follows: bonding pads 13a in the processing part 12a are respectively **connected** with inner leads 14 via Au bonding wires 15 of a diameter of 38.mu.m or thereabouts and if the power part 12b comprises, for example, a power MOSFET having characteristics that the value of a source/**drain** breakdown strength is 50V or larger, the value of a current capable of outputting continuously is 4A or thereabouts and an ON resistance value is about 0.22.OMEGA. or smaller, a pad 13b, which used as an output end, in the power part 12b is **connected** to an inner lead 14 via an Al wire 16 of a diameter of 250.mu.m or thereabouts.

L14 ANSWER 18 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1989-239447 JAPIO
TI FET SOLUTION COMPONENT SENSOR
IN UNO SHIGEKI; SAKAI TADASHI
PA TOSHIBA CORP, JP (CO 000307)
PI JP 01239447 A 19890925 Heisei
AI JP1988-65674 (JP63065674 Heisei) 19880322
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 978, Vol. 13, No. 572, P. 14 (19891218)
AB PURPOSE: To prevent the infiltration of water and moisture into electrode

parts and to improve reliability by forming the sensitive **gates**, electrode pads and leads of FET elements to an opposite surface and molding the pads and leads by using a frame and resins.
CONSTITUTION: Islands 2 of silicon are formed by etching the upper silicon layer of a silicon **wafer**. The electrode pads 3, 3' of the **drains** and sources of the FET elements are provided on the islands 2 and further, the sensitive **gates** are provided to the base of the islands 2 to form **chips**. **Chip** holding holes 13 and leads 12 are previously provided on the substrate 11 and the **chips** are installed in the holes 13 to electrically **connect** the pads 3, 3' and the **leads** 12. The **frame** 14 larger than the holes 13 are thereafter placed on the **chips** and the silicone resin and epoxy resin are packed into the frame. Since the pads and leads are provided on the surface opposite to the sensitive **gates**, the immersion of the pads and leads in a soln. is obviated and the infiltration of the water and moisture is prevented by the frame and the packed resins. The reliability is thus improved.

L14 ANSWER 19 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1987-274645 JAPIO
TI **LEAD FRAME** AND ELECTRONIC DEVICE USING THE SAME
IN HOTTA KIYOMICHI
PA HITACHI LTD, JP (CO 000510)
PI JP 62274645 A 19871128 Showa
AI JP1986-117249 (JP61117249 Showa) 19860523
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 609, Vol. 12, No. 162, P. 121 (19880517)
AB PURPOSE: To make it possible to utilize one **lead frame** for multiple purposes, by forming the second lead part and the third lead part, in which one end is **connected** to a semiconductor **chip** through a wire and the other end part becomes an outer **connecting** terminal, at facing positions as a unitary body through the first lead part.
CONSTITUTION: When a **lead frame** is used for a bipolar transistor, a semiconductor **chip** A is fixed to a fixing part 24a. The base terminal of the semiconductor **chip** A is **connected** to, e.g., a lead part23 through a wire. The emitter terminal of the **chip** A is **connected** to, e.g., a lead terminal part 25 through a wire. Then, a lead part 24 becomes a collector. When the frame is utilized in an MOSFET, a semiconductor **chip** B for the MOSFET is fixed to a fixing part 23a of the first lead part 23. The **drain** terminal of the semiconductor **chip** B is **connected** to the lead part 24 or to the lead part 25 through a wire 6A. The **gate** terminal of the semiconductor **chip** B is **connected** to the lead part 24 or to the lead part 25 through the wire 6A.

L14 ANSWER 20 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1986-237455 JAPIO
TI MOLDED ELECTRICAL PART
IN KANAZAWA MASAYOSHI
PA SONY CORP, JP (CO 000218)
PI JP 61237455 A 19861022 Showa
AI JP1985-80028 (JP60080028 Showa) 19850415
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 489, Vol. 11, No. 83, P. 41 (19870313)
AB PURPOSE: To reduce parasitic capacitance by a resin by each forming a semiconductor **chip**, a first resin layer sealing the semiconductor **chip** and a second resin layer shaped outside the

first resin layer and making the permittivity of the first resin layer smaller than that of the second resin layer.
CONSTITUTION: **Lead frames** 3, 4 are fitted symmetrically on both sides of a **lead frame** 2 to which a GaAs **chip**, to which a GaAsFET is shaped, is **mounted** on the same plane as the **lead frame** 2, and source pads for the **chip** 1 and the frame 2 are **connected** by bonding wires 5, 6, a **gate** pad for the **chip** 1 and the frame 3 by a bonding wire 7 and a **drain** pad for the **chip** 1 and the frame 4 by a bonding wire 8 respectively. These **chip** 1, wires 5-8, central section of the frame 2 and one end sections of the frames 3, 4 are molded to a square-shaped external form by a Teflon group BT resin 9 as a low permittivity resin, and the outside of the resin 9 is molded to the same square-shaped external form as the resin 9 by epoxy resin 10.

L14 ANSWER 21 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1985-037758 JAPIO
TI SEMICONDUCTOR DEVICE
IN OGAWA YOSHITO
PA NEC CORP, JP (CO 000423)
PI JP 60037758 A 19850227 Showa
AI JP1983-145930 (JP58145930 Showa) 19830810
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 326, Vol. 9, No. 1591, P. 97 (19850704)
AB PURPOSE: To miniaturize the titled device by fixing semiconductor **chips** on front and back surfaces of a **lead frame** , respectively.
CONSTITUTION: **Gate** electrode leads 4 and 8 of the **lead frame** to which a semiconductor **chip** is fixed are **joined** to each other, and leads 5 and 9 arranged between the leads 4 and 8 and **drain** leads 6 and 10 and then shielding them are also **joined**. The semiconductor **chip** 1 is fixed to the surface, and the source and **drain** electrodes are **connected** to the leads 3 and 6. The semiconductor **chip** 2 is fixed to the back of the section with the **chip** 1 fixed, the source and **drain** electrodes being **connected** to the leads 7 and 10, and both the **chips** and the **connections** being then resin-sealed 11. This construction makes it sufficient that the area of the **chip mounted** section is that for a piece,and enables the intersection of **connections** in proper use of the front and back surfaces, resulting in the excellent heat balance betwen the **chips**, accordingly the multi-**chip** type device can be miniaturized.

L18 ANSWER 1 OF 1 WPIX (C) 2002 THOMSON DERWENT
AN 1993-241325 [30] WPIX
DNN N1993-185662
TI Stable voltage source for different type **microelectronic** devices - has gate of first transistor **connected** to substrate of second transistor, whose **drain** is **connected** to second lead of reference voltage source.
DC U24
IN GROMOV, I S; IGUMNOV, D V; SHCHERBAKOVA, S N
PA (MORA-R) MOSC RADIO ELTRN AUTOM INST
CYC 1
PI SU 1749888 A1 19920723 (199330)* 3p
ADT SU 1749888 A1 SU 1990-4833944 19900601
PRAI SU 1990-4833944 19900601
AB SU 1749888 A UPAB: 19931118
The voltage source includes IGFETs (1,4) with n-channels, bias (2) and ballast (3) resistors, and voltage reference element consisting of single diode or several ones (5,6) **connected** in series.
Connection of the first IGFET (1) and resistor (3) between the input and output leads, the second IGFET (4) and voltage reference element between the output **lead** and common **rail** allows limitations on upper level of output voltage to be reduced.
USE/ADVANTAGE - In secondary power sources of radioelectronic equipment. Wider working range of output voltage.
Bul.27/23.7.92
Dwg.1/1

L25 ANSWER 1 OF 1 JAPIO COPYRIGHT 2002 JPO
AN 1997-213840 JAPIO
TI RESIN-SEALED TYPE SEMICONDUCTOR DEVICE
IN KAMIMURA KAZUYOSHI
PA NEC CORP, JP (CO 000423)
PI JP 09213840 A 19970815 Heisei
AI JP1996-14972 (JP08014972 Heisei) 19960131
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 97, No. 8
AB PURPOSE: TO BE SOLVED:To improve a high-frequency characteristic even in the **mounting** of the semiconductor **chip** of an FET having a cavity right under a **gate** electrode by forming a recessed part in the lead of a **lead frame**, **mounting** the semiconductor **chip** so that the **active region** is opposite to the recessed part and hollowing the part on the **active region**.
CONSTITUTION: ad frame having a **frame** part and **leads** 1, 2, 3 is formed. A recessed part 3a is formed in the central part of the lead 3. A semiconductor **chip** 6 is positioned to the **lead frame** and **mounted** thereon so that a **gate** pad is located on the lead 1, a **drain** pad is located on the lead 2 and a source pad is located on the lead 3 and that an FET part is located on the recessed part 3a to braze the electrodes of the semiconductor **chip** 6 on the leads 1 to 3. When the **lead frame** on which the semiconductor **chip** 6 is **mounted** is sealed with a resin after cooled, air inside the recessed part 3 prevents a resin from entering the recessed part 3a, so that the increase of capacity due to the resin may be suppressed.

L26 ANSWER 1 OF 4 WPIX (C) 2002 THOMSON DERWENT
AN 1993-295232 [37] WPIX
DNN N1993-227487 DNC C1993-130973
TI Integrated photoelectric receiving device mfr. - has a PIN-type photodetector and a FET junction integrated in a single **chip**.
DC A85 G06 L03 U11 U13
IN LEE, Y; OH, K
PA (KANK-N) ZH KANKOKU DENSHI TSUSHIN KENKYUSHO; (KOEL-N) KOREA ELECTRONICS & TELECOM RES; (ELTE-N) ELECTRONICS & TELECOM RES INST
CYC 3
PI US 5242839 A 19930907 (199337)* 12p
JP 05226598 A 19930903 (199340) 9p
KR 9500522 B1 19950124 (199645)
ADT US 5242839 A US 1992-981865 19921125; JP 05226598 A JP 1992-314764 19921125; KR 9500522 B1 KR 1991-21083 19911125
PRAI KR 1991-21083 19911125
AB US 5242839 A UPAB: 19931123
Mfr. of an integrated photoelectric receiving device having a photodetector and a transistor formed on a semi-dielectric substrate, comprises: (a) etching a photodetector forming area of a predetermined depth on the substrate by using a selective etchant; (b) sequentially forming an n-type channel layer, an etchant stopper layer and an absorption layer on the substrate etched; (c) removing the absorption layer excluding the photodetector forming area by the selective etchant; (d) sequentially removing the etchant stopper layer and the type n-channel layer between the photodetector and the transistor forming areas to electrically insulate the photodetector and the transistor; (e) sequentially forming a p-type InP layer and a p-type InGaAs layer on the entire surface of the substrate exposed; (f) selectively etching the p-type InGaAs layer positioned on the photodetector forming area by a lithography process using a sensitive material as an etching mask; (g) forming p-type electrodes on the p-type InP layer defined on the photodetector forming area and the p-type InGaAs layer in the transistor forming area, respectively; (h) masking the photodetector forming area by lithography process using the sensitive material as an etching mask and removing the p-type InGaAs layer, the p-type InP layer and the etching stopper layer by using the p-type **gate** electrode as a mask; (i) depositing n-type metal layer on the n-type channel layer and any one of the p-type electrodes and forming an ohmic contact of a source and **drain** of the photodetector and the transistor; (j) coating a polyimide layer on the entire structure and etching the polyimide layer on the electrode forming portion and photoabsorption portion of the photodetector and the source and **drain** forming portions of the transistor; forming wiring metal layers on the electrode portions of the photodetector and the source and **drain** forming portions of the transistor.
USE/ADVANTAGE - Device has improved receiving sensitivity and operating speed. The device comprises a PIN type photodetector and a junction FET integrated on a single **chip** for economical and simplified fabrication.
11
Dwg. 3/3

L26 ANSWER 2 OF 4 WPIX (C) 2002 THOMSON DERWENT
AN 1993-090176 [11] WPIX
DNN N1993-068714 DNC C1993-040470
TI Sealing **die** appts. forming resin package of semiconductor

chip and **lead frame** - with **die** cavity with charging port for molten resin, with separate resin **drain gate** for efficient filling, and pot to store drained resin.
DC A85 L03 U11
PA (SHIA) SHINKO DENKI KOGYO KK
CYC 1
PI JP 05036745 A 19930212 (199311)* 4p
ADT JP 05036745 A JP 1991-216407 19910801
PRAI JP 1991-216407 19910801
AB JP 05036745 A UPAB: 19931112
A semiconductor **chip** and part of **lead frame** are sealed by charging a molten resin into the cavity of a **die** through a resin entrance **gate**. A resin **drain gate** to **drain** a part of the charged resin from the cavity is disposed at a different position from the position of the entrance **gate**, and a resin pot is formed to store the drained resin. USE/ADVANTAGE - For making semiconductor device packages of 1mm or less in thickness. Owing to the resin **drain gate**, the resin is fully charged in the cavity.
1/4
Dwg.1/4

L26 ANSWER 3 OF 4 WPIX (C) 2002 THOMSON DERWENT
AN 1987-105220 [15] WPIX
TI Frequency performance **IC lead frame** - has grounded source between **gate** input and **drain** output terminals to prevent signal leaking NoAbstract Dwg 3/3.
DC U11
PA (HITA) HITACHI LTD
CYC 1
PI JP 62052950 A 19870307 (198715)* 10p
ADT JP 62052950 A JP 1985-191912 19850902
PRAI JP 1985-191912 19850902

L26 ANSWER 4 OF 4 JAPIO COPYRIGHT 2002 JPO
AN 1981-165328 JAPIO
TI SEMICONDUCTOR DEVICE
IN SHIBATA TAKASHI
PA HITACHI LTD, JP (CO 000510)
PI JP 56165328 A 19811218 Showa
AI JP1980-68958 (JP55068958 Showa) 19800526
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 100, Vol. 6, No. 521, P. 73 (19820407)
AB PURPOSE: To prevent the resistance fall of the substrate for a semiconductor element by a method wherein a high resistance semiconductor layer, whereon an element region will be formed, is formed on a low resistance semiconductor substrate and a around pad is provided in such manner that a part of which comes in contact with the low resistance semiconductor substrate.
CONSTITUTION: On the upper surface of the low resistance semiconductor substrate 18 having the resistivity of 0.1.OMEGA./cm or below, the high resistance semiconductor layer 19 of 6-15.mu.m in thickness having the resistivity of 1-15.OMEGA./cm, is formed and on this high resistance semiconductor layer 19, a source 20, a **drain** 21 and **gates** 22 and 23, to be used as the element region whereon an MOS will be constituted, for example, are provided. Subsequently, wirings 27 and 28 and the ground pad 26 are formed. At this time, a part 31 of the ground pad 26 is constituted in such manner that it penetrates the high

resistance semiconductor layer and is conducted to the low resistance semiconductor substrate 18. Through these procedures, no resistance fall of the substrate is generated even when a semiconductor **chip** is bonded on a **lead frame** using a high resistance adhesive material 7.

=> D BIB AB 1-34

L31 ANSWER 1 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 2002-215536 [27] WPIX
CR 1991-230305 [31]; 1993-395456 [49]; 1994-135001 [16]; 1997-558377 [51]; 2001-089780 [56]; 2002-129146 [14]
DNN N2002-165094
TI Semiconductor **die** system has on-**chip** capacitor operably **coupled** between **active** substrate **areas** and carrier substrate to provide filtering capacitance for semiconductor **die**.
DC U11
IN CHERN, W; DUESMAN, K G; JOHNSON, G M; NEVILL, L R; PARKINSON, W D; PROTIGAL, S N; TRENT, T M
PA (CHER-I) CHERN W; (DUES-I) DUESMAN K G; (JOHN-I) JOHNSON G M; (NEVI-I) NEVILL L R; (PARK-I) PARKINSON W D; (PROT-I) PROTIGAL S N; (TREN-I) TRENT T M
CYC 1
PI US 2001042899 A1 20011122 (200227)* 12p
ADT US 2001042899 A1 CIP of US 1988-200673 19880531, Cont of US 1988-291294 19881227, Cont of US 1991-774121 19911008, Cont of US 1993-34001 19930319, Cont of US 1994-178716 19940110, Cont of US 1996-671248 19960627, Cont of US 1997-965741 19971107, US 2001-776387 20010202
FDT US 2001042899 A1 Cont of US 5307309, Cont of US 5687109, Cont of US 6184568
PRAI US 1988-291294 19881227; US 1988-200673 19880531; US 1991-774121 19911008; US 1993-34001 19930319; US 1994-178716 19940110; US 1996-671248 19960627; US 1997-965741 19971107; US 2001-776387 20010202
AB US2001042899 A UPAB: 20020429
NOVELTY - The system has a semiconductor **die** (11) operably **coupled** to a carrier substrate and having a semiconductor substrate having **active** substrate **areas**. A portion of an on-**chip** capacitor is formed in one **active** substrate **area** of semiconductor substrate. The on-**chip** capacitor is operably **coupled** between **active** substrate **areas** and carrier substrate to provide filtering capacitance for semiconductor **die**.

USE - Semiconductor **die** system.

ADVANTAGE - Reduces the transmission of voltage transients on the semiconductor **die**. Offers a semiconductor **die** system which can be manufactured easily.

DESCRIPTION OF DRAWING(S) - The figure shows the equivalent circuit of the semiconductor circuit device **connected** through a **lead frame connection** wire and having an on-**chip** decoupling capacitor.

Semiconductor **die** 11

Dwg.3/12

L31 ANSWER 2 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 2002-153689 [20] WPIX
DNN N2002-116839 DNC C2002-047966
TI **Lead frame** for **attachment** to semiconductor **chip** in leads-over-**chip** assembly, comprises electrically insulative material layer bonded to portion of bus bar not **connected** to **active area** of semiconductor **die**.
DC A85 L03 U11
IN COURTENAY, R W

PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 6255720 B1 20010703 (200220)* 13p
ADT US 6255720 B1 Cont of US 1997-872403 19970610, US 1998-70464 19980430
FDT US 6255720 B1 Cont of US 5780923
PRAI US 1997-872403 19970610; US 1998-70464 19980430
AB US 6255720 B UPAB: 20020402

NOVELTY - A **lead frame** comprises:

(A) a **lead frame** pattern having **leads** including lead fingers and a bus bar which has at least a portion of its lower surface for insulative **attachment** to at least a portion of the active surface of a semiconductor **die**; and

(B) a layer of electrically insulative material bonded to at least a portion of the upper surface of the bus bar.

DETAILED DESCRIPTION - A **lead frame** for electrical **connection** to a semiconductor **die** (12) which has an active surface (14) having bond pads (16) comprises a **lead frame** pattern having **leads** (18) including lead fingers (18A) and a bus bar (20). The bus bar has at least a portion of its lower surface for insulative **attachment** to at least a portion of the active surface of the **die**. A layer of electrically insulative material is bonded to at least a portion of the upper surface of the bus bar, portions of the upper surface of the bus bar for **connecting** to bond pads and portions of the upper surface of the bus bar insulated from the **die**. The layer of electrically insulative material bonded to at least a portion of the upper surface of the bus bar comprises tape, hardenable fluid, or paste. INDEPENDENT CLAIMS are also included for:

(A) a method for making a **lead frame** for conductive bonding to a semiconductor **die** comprising forming a lead pattern on a conductive metal, bonding a layer of electrically insulative material to a portion of the upper surface of the conductive metal which is configured to comprise a portion of bus bars, and removing the electrically insulative material from wire bonding areas (44) on the upper surface of the bus bars; and

(B) a semiconductor assembly comprising a semiconductor **die**, a first layer of insulative material (24) covering a portion of the active surface of the **die**, the **lead frame**, conductive wires (34, 42) **connecting** bond pads to lead fingers and **connecting** bond pads to conductive bus bars, and a second layer of electrically insulative material (50) secured to at least a portion of the upper surface of the conductive bus bars.

USE - For **attachment** to semiconductor **chip** in leads-over-**chip** (LOC) assembly.

ADVANTAGE - The method provides an improvement in the construction of semiconductor devices. It avoids inadvertent shorting of the wires to the bus bars. Looping heights and wire lengths are reduced so that subsequent wire sweep during encapsulation is avoided.

DESCRIPTION OF DRAWING(S) - The figure shows a perspective view of a semiconductor device of the invention.

Semiconductor **die** 12
Active surface 14
Bond pads 16
Leads 18
Lead fingers 18A
Bus bar 20
First layer of insulative material 24
Conductive wires 34, 42
Wire bonding areas 44

Second layer of electrically insulative material 50
Dwg.1/5

L31 ANSWER 3 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 2002-088131 [12] WPIX
TI Method for manufacturing dual **die** package.
DC U11
IN KWAK, M G
PA (SMSU) SAMSUNG ELECTRONICS CO LTD
CYC 1
PI KR 2001076670 A 20010816 (200212)* 1p
ADT KR 2001076670 A KR 2000-3957 20000127
PRAI KR 2000-3957 20000127
AB KR2001076670 A UPAB: 20020221
NOVELTY - A method for manufacturing a dual **die** package is provided to proceed the **coupling** process of the leads of the first **lead frame** and the second lead from with a conductive film to simplify the manufacturing process.
DETAILED DESCRIPTION - The dual **die** package manufacturing method includes following steps. At first, the first **lead frame**(40) including the first lead which includes the first **coupling** member and the first junction member and the first damper. At second, the second **lead frame** including the second lead which includes the second **coupling** member and the second junction member and the second damper. At third, the first and the second **lead frames** are **coupled** with each other by applying conductive film between them. At last, a resin is filled to seal a region where the first and the second semiconductor **chips** are implemented to form a package body. The first **coupling** member is located on an **active region** of the first semiconductor **chip**. The first damper which is formed in a direction penetrating the first junction member in perpendicular. The second damper which is formed in a direction penetrating the second junction member in perpendicular.
Dwg.1/10

L31 ANSWER 4 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 2001-048911 [06] WPIX
CR 1998-541884 [46]
DNN N2001-037455 DNC C2001-013283
TI Semiconductor device for use in portable electronics apparatus comprises diverse semiconductor **die** fixed to a common **lead frame** and within a common package or housing.
DC A85 L03 U11 U13 U24
IN CHEAH, C; DAVIS, C; KINZER, D M
PA (INRC) INT RECTIFIER CORP
CYC 1
PI US 6133632 A 20001017 (200106)* 10p
ADT US 6133632 A Provisional US 1996-29483P 19961024, Cont of US 1997-816829 19970318, US 1998-161790 19980928
FDT US 6133632 A Cont of US 5814884
PRAI US 1996-29483P 19961024; US 1997-816829 19970318; US 1998-161790 19980928
AB US 6133632 A UPAB: 20020402
NOVELTY - A semiconductor device comprises, in combination, first and second semiconductor **die** having opposing surfaces which contain electrodes. A thin conductive **lead frame** has a common main pad area having first parallel pins integral with and extending from one edge and second pins separated from the common main pad area. A molded

housing encapsulates the **lead frame** and the **die**.

DETAILED DESCRIPTION - A semiconductor device comprises, in combination, first and second semiconductor **die** having opposing surfaces which contain electrodes. A thin conductive **lead frame** has a common main pad area having first parallel pins (1-4) integral with and extending from one edge and second pins (5-8) separated from the common main pad area. The second pins are disposed along an edge of the common main pad area opposite to the side containing the first pins. At least two of the second pins are electrically **connected** together. One of the opposing surfaces of each of the first and second **die** is disposed atop and in electrical contact with the common main pad area. The opposite one of the opposing surfaces of the first and second **dies** are in electrical contact with the pin(s). A molded housing (30) encapsulates the **lead frame** and the first and second **die**. The first and second pins extend beyond the boundary of the molded housing and available for external **connection**.

USE - For use in portable electronics apparatus.

ADVANTAGE - The device improves efficiency of a direct current to direct current converter by reducing power **drain** on batteries, leading to a longer life. For desk top systems, the device reduces power dissipation and heat generation near temperature-sensitive parts, e.g. microprocessors. The device also provides substantial savings in board space while reducing component count and assembly costs.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic top view of the package.

Pins 1-8

MOSFET **die** 10

Schottky **die** 12

Housing 30

Dwg.4/9

L31 ANSWER 5 OF 34 WPIX (C) 2002 THOMSON DERWENT

AN 2000-184763 [17] WPIX

DNN N2000-136462

TI Low power packaging design for surface **mount** power MOSFET device has **drain connectors** formed from a punched metal **leadframe** sheet.

DC U11 U12

IN HEWITT, C

PA (HARO) HARRIS CORP

CYC 26

PI EP 978871 A2 20000209 (200017)* EN 8p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
JP 2000082816 A 20000321 (200025) 7p

ADT EP 978871 A2 EP 1999-114184 19990722; JP 2000082816 A JP 1999-221075 19990804

PRAI US 1998-129321 19980805

AB EP 978871 A UPAB: 20000405

NOVELTY - A **connector** (20) has a strap (21) for a **drain** contact in a **leadframe** metal sheet. Edge tab contacts (22,24) are formed by punching the sheet to enable surface **mounting** of the device. **Drain** electrical current from the backside of the **mounted** device is passed to the topside via the bent edge tabs. The package is known as a StrapPak package.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) a method for flip-**chip mounting** a semiconductor MOSFET device.

(b) a method for simultaneously **mounting drain connectors** on a number of MOSFETs.

USE - Packaging for power metal-oxide-semiconductor field-effect transistors (MOSFETs) for use as power supplies in e.g. laptop computers, personal organizers or cellular telephones.

ADVANTAGE - The package significantly reduces the contribution to the overall component resistance and hence the power loss in the on state. Packages are smaller, cheaper to produce and compatible with conventional PCB assembly equipment.

DESCRIPTION OF DRAWING(S) - The figure shows an expanded view of a portion of the metal sheet showing a **drain connector**.

Connector 20

Strap 21

Edge tab contacts 22,24

Dwg.2/9

L31 ANSWER 6 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1999-620825 [53] WPIX
DNN N1999-457882
TI Passively aligned optoelectronic **coupling** assembly for optical communication.
DC P81 V07
IN MOORE, A J
PA (CIEL-N) CIELO COMMUNICATIONS INC
CYC 86
PI WO 9954762 A1 19991028 (199953)* EN 28p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ UG ZW
W: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZA ZW
US 6015239 A 20000118 (200011)
AU 9938639 A 19991108 (200014)
EP 1086392 A1 20010328 (200118) EN
R: DE FR GB
KR 2001042888 A 20010525 (200168)
ADT WO 9954762 A1 WO 1999-US8670 19990420; US 6015239 A US 1998-63122 19980420; AU 9938639 A AU 1999-38639 19990420; EP 1086392 A1 EP 1999-921417 19990420, WO 1999-US8670 19990420; KR 2001042888 A KR 2000-711673 20001020
FDT AU 9938639 A Based on WO 9954762; EP 1086392 A1 Based on WO 9954762
PRAI US 1998-63122 19980420
AB WO 9954762 A UPAB: 19991215
NOVELTY - Package of vertical cavity surface emitting laser (VCSEL) (28) consists of **lead frame** (24) with **die** pad (26) on which VCSEL is **mounted** and is covered by transparent enclosure (34). Frusto-conical section (20) formed in the enclosure is received inside a frusto-conical cavity (18) of light guide end housing (14) for aligning light **active area** of VCSEL with end of light guide in housing.

DETAILED DESCRIPTION - The alignment takes place automatically when the frusto-conical section of enclosure is inserted in frusto-conical cavity of light guide end housing. In the inserted condition, relative rotation between the package and housing is enabled.

USE - For optical communication.

ADVANTAGE - Since passive alignment is used, need for manual

aligning is avoided, thus allowing quick optical **coupling** between VCSEL and light guide. Number of components used is minimum and hence structure is simplified. Assembly of light guide end housing to the optical fiber is easy. The housing can be used to accommodate any type of cable. The **coupling** is compatible with individual or arrayed light sources with plastic encapsulation.

DESCRIPTION OF DRAWING(S) - The figure is a sectional view of **coupling** arrangement.

Housing 14

Frusto-conical cavity 18

Frusto-conical section 20

Lead frame 24

Die pad 26

VCSEL 28

Transparent enclosure 34

Dwg.4/14

L31 ANSWER 7 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1999-358951 [31] WPIX
DNN N1999-267262
TI EMC optimised power switch especially MOS power transistor - has first terminal for active potential and second terminal for rest potential and **lead frame** is **connected** to second terminal.
DC U11 U12 U13 U21
IN GASSEL, H; GAUTIOLER, J; KLOTZ, F; MAERZ, M; GANTIOLER, J
PA (SIEI) SIEMENS AG
CYC 20
PI DE 19806817 C1 19990708 (199931)* 6p
WO 9943027 A1 19990826 (199942) DE
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: JP US
EP 976154 A1 20000202 (200011) DE
R: DE FR GB IE IT
JP 2001520810 W 20011030 (200202) 14p
ADT DE 19806817 C1 DE 1998-19806817 19980218; WO 9943027 A1 WO 1999-DE193 19990126; EP 976154 A1 EP 1999-908750 19990126, WO 1999-DE193 19990126; JP 2001520810 W JP 1999-541954 19990126, WO 1999-DE193 19990126
FDT EP 976154 A1 Based on WO 9943027; JP 2001520810 W Based on WO 9943027
PRAI DE 1998-19806817 19980218
AB DE 19806817 C UPAB: 19990806

The power switch includes a semiconductor **chip** (3) on a lead frame (2). The **chip** (3) has at least a first terminal (D,K) for an active potential and a second terminal (S,A) for a quiescent potential. The **lead frame** (2) is **connected** to the second terminal (S,A).

Preferably the first terminal is the **drain** and the second terminal is the source of a transistor (6). Alternatively the first terminal is the cathode and the second terminal is the anode of a diode. The **chip** may be **mounted** over the source(s) of the transistor on the **lead frame** (2). A control terminal (G) of the transistor (6) may be **connected** via trenches in the **chip** (3) to the free surface of the **chip**.

USE - For all power transistors.

ADVANTAGE - Interrupts asymmetrical interferences with simultaneous

reduction in circuit cost and complexity.
Dwg.1/4

L31 ANSWER 8 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1998-439632 [38] WPIX
DNN N1998-342613
TI Anti-tamper shield for **integrated circuit** used in cable and satellite TV decoder - includes bond wire carried within and/or proximate to encapsulating layer such that decapsulation of **IC** will cause rupture of electrically conductive member, thus, rendering processor non-functional.
DC T01 U11 U14
IN CANDELORE, B
PA (GENN) GEN INSTR CORP DELAWARE; (GENN) GEN INSTR CORP
CYC 31
PI EP 860882 A2 19980826 (199838)* EN 11p
R: AL AT BE CH DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
CA 2230065 A 19980824 (199903)
JP 10294325 A 19981104 (199903) 42p
US 5861662 A 19990119 (199911)
CN 1200570 A 19981202 (199916)
KR 98071653 A 19981026 (199953)
MX 9801450 A1 19990101 (200051)
TW 388942 A 20000501 (200062)
ADT EP 860882 A2 EP 1998-103099 19980221; CA 2230065 A CA 1998-2230065 19980220; JP 10294325 A JP 1998-82375 19980224; US 5861662 A US 1997-804792 19970224; CN 1200570 A CN 1998-107718 19980224; KR 98071653 A KR 1998-5771 19980224; MX 9801450 A1 MX 1998-1450 19980223; TW 388942 A TW 1998-102495 19980221
PRAI US 1997-804792 19970224
AB EP 860882 A UPAB: 19980923
The shield (230) includes a bond wire (270) which passes through a protective layer such as an epoxy encapsulating layer of an **IC** (200). The bond wire carries a signal, such as a steady state current, which allows an active component of the **IC**, such as a secure processor, to function. The bond wire is carried within and/or proximate to the encapsulating layer such that a decapsulation of the **IC** will cause a rupture of the electrically conductive member, thus, rendering the processor non-functional.

The bond wire may be **coupled** to the processor in a variety of configurations, including the use of internal or external bond pads, **lead frame** contacts, and/or directly to a computer board on which the **IC** is carried. A metallic shield layer may be located between the active component and a top portion of the encapsulating layer to prevent a pirate from using an electron microscope, for example, to survey the **active** component **region**.

ADVANTAGE - Deters or otherwise hinders probing of **IC** by pirate, and is compatible with existing **chip** design and inexpensive to implement.
Dwg.2/4

L31 ANSWER 9 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1998-368543 [32] WPIX
DNN N1998-288520
TI LOC type semiconductor package manufacturing method - involves **coupling** electrode pad of semiconductor **chip** and inner **leads** of **lead frame**, electrically.
DC U11

PA (SMSU) SAMSUNG ELECTRONICS CO LTD
CYC 1
PI JP 10144703 A 19980529 (199832)* 11p
ADT JP 10144703 A JP 1996-296747 19961108
PRAI JP 1996-296747 19961108
AB JP 10144703 A UPAB: 19980812
The method involves arranging several semiconductor **chips** (126) on a **wafer** (120) which is positioned in a movable stage. The semiconductor **chip** comprises several electrode pads with the **active area** at the centre surface. A lead bonding area is formed at both sides of the electrode pad and a protective layer is formed at the upper surface of the **wafer**.

The semiconductor **chip** is isolated from the **wafer** and is **connected** with an external circuit through a **lead frame**. The electrode pad of the semiconductor **chip** is **coupled** electrically with the inner **leads** of **lead frame** and the **die**-bonding stage is **coupled** with the **active area** of the **chip**.

ADVANTAGE - Avoids use of polyamide adhesive layer. Enables adjustment of size and thickness of adhesive layer. Improves reliability of package element.
Dwg.2/14

L31 ANSWER 10 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1996-474339 [47] WPIX
DNN N1996-400195
TI Low-power semiconductor **integrated circuit** with analogue circuit - has carrier recombination layer formed at one corner of silicon substrate using charge irradiation or gold diffusion, sepg. substrate into two partial circuits.
DC U13
PA (HITA) HITACHI LTD
CYC 1
PI JP 08241960 A 19960917 (199647)* 7p
ADT JP 08241960 A JP 1995-45259 19950306
PRAI JP 1995-45259 19950306
AB JP 08241960 A UPAB: 19961124
The **integrated circuit** has bonding putts (8) along two sides of its silicon substrate (2). The putts are **connected** by bonding wires (4) to **lead frames** (3).

A carrier recombination layer (1) is formed by golden diffusion or charge irradiation at one corner of the substrate. The layer forms two partial circuits on the substrate. A back-side electrode (5) is provided after **lead frame** to which the layer is terminated.

ADVANTAGE - Ensures constant substrate potential because bonding wire is not required with provision of backside electrode and because substrate and **drain** power supplies are sepd.; suppresses two kinds of noises generated in substrate; reduces probability of incorrect semiconductor **integrated circuit** operation caused by substrate noise.
Dwg.1/14

L31 ANSWER 11 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1996-259628 [26] WPIX
CR 1999-189096 [16]; 1999-560965 [47]; 2001-070049 [04]
DNN N1996-218422
TI Cleaning method for raw semiconductor **wafers** and **lead frames** - by immersing **wafer** in deionised water and

draining with water replaced by carrier gas containing leaning enhancement material.

DC P43 U11

IN ANDERSON, J H; BHUSHAN, A; BHUSHAN, R; MOHINDRA, R; NOWELL, J; PURI, S; WONG, D C

PA (YIEL-N) YIELD-UP INT CORP; (YIEL-N) YIELDUP INT CORP; (YIEL-N) YIELDUP INT; (SCDM-N) SCD MOUNTAIN VIEW

CYC 66

PI WO 9614944 A1 19960523 (199626)* EN 46p
RW: AT BE CH DE DK ES FR GB GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG
W: AM AT AU BB BG BR BY CA CH CN CZ DE DK EE ES FI GB GE HU IS JP KE KG KP KR KZ LK LR LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TT UA UG UZ VN
AU 9641594 A 19960606 (199637)
US 5571337 A 19961105 (199650) 18p
US 5634978 A 19970603 (199728) 13p
EP 800424 A1 19971015 (199746) EN
R: DE FR GB IT
US 5685327 A 19971111 (199751) 16p
US 5772784 A 19980630 (199833)
JP 10508986 W 19980902 (199845) 49p
KR 97706916 A 19971201 (199847)
US 5868150 A 19990209 (199913)
US 5878760 A 19990309 (199917)
US 5891256 A 19990406 (199921)
US 5932027 A 19990803 (199937)
US 5988189 A 19991123 (200002)
US 6352082 B1 20020305 (200224)

ADT WO 9614944 A1 WO 1995-US14832 19951113; AU 9641594 A AU 1996-41594 19951113; US 5571337 A CIP of US 1994-339326 19941114, US 1995-437541 19950509; US 5634978 A US 1994-339326 19941114; EP 800424 A1 EP 1995-939961 19951113, WO 1995-US14832 19951113; US 5685327 A CIP of US 1994-339326 19941114, Div ex US 1995-437541 19950509, US 1996-695285 19960808; US 5772784 A CIP of US 1994-339326 19941114, CIP of US 1995-437541 19950509, US 1995-555634 19951108; JP 10508986 W WO 1995-US14832 19951113, JP 1996-516300 19951113; KR 97706916 A WO 1995-US14832 19951113, KR 1997-703216 19970513; US 5868150 A CIP of US 1994-339326 19941114, CIP of US 1995-437541 19950509, Div ex US 1995-555634 19951108, US 1997-862082 19970522; US 5878760 A CIP of US 1994-339326 19941114, CIP of US 1995-437541 19950509, Div ex US 1995-555634 19951108, US 1997-862083 19970522; US 5891256 A CIP of US 1994-339326 19941114, CIP of US 1995-437541 19950509, Cont of US 1995-555634 19951108, US 1997-861456 19971229; US 5932027 A CIP of US 1994-339326 19941114, CIP of US 1995-437541 19950509, Cont of US 1995-555634 19951108, US 1998-5976 19980112; US 5988189 A CIP of US 1994-339326 19941114, CIP of US 1995-437541 19950509, Cont of US 1995-555634 19951108, Cont of US 1996-710701 19960919, US 1998-111149 19980706; US 6352082 B1 CIP of US 1994-339326 19941114, CIP of US 1995-437541 19950509, Div ex US 1995-555634 19951108, Cont of US 1997-862083 19970522, US 1998-157765 19980921

FDT AU 9641594 A Based on WO 9614944; EP 800424 A1 Based on WO 9614944; US 5685327 A Div ex US 5571337; US 5772784 A CIP of US 5571337, CIP of US 5634978; JP 10508986 W Based on WO 9614944; KR 97706916 A Based on WO 9614944; US 5868150 A CIP of US 5571337, CIP of US 5634978, Div ex US 5772784; US 5878760 A CIP of US 5571337, CIP of US 5634978, Div ex US 5772784; US 5891256 A CIP of US 5571337, CIP of US 5634978, Cont of US 5772784; US 5932027 A CIP of US 5571337, CIP of US 5634978, Cont of US 5772784; US 5988189 A CIP of US 5571337, CIP of US 5634978, Cont of US

5772784; US 6352082 B1 CIP of US 5571337, CIP of US 5634978, Div ex US 5772784, Cont of US 5878760
PRAI US 1995-555634 19951108; US 1994-339326 19941114; US 1995-437541 19950509; US 1996-695285 19960808; US 1997-862082 19970522; US 1997-862083 19970522; US 1997-861456 19971229; US 1998-5976 19980112; US 1996-710701 19960919; US 1998-111149 19980706; US 1998-157765 19980921
AB WO 9614944 A UPAB: 20020416
The method uses a mixt. of water and gas cleaning. The **wafer** is moved from an acid etch (410) to a rinse stage. This uses deionised water (430) to remove the acid from the **wafer**. The water can be partially dumped (44) into a bottom **drain**. During this dumping an ultra pure, non-reactive gas replaces the water.

Clean deionised water then covers the **wafer** surface area.

When the acid is largely removed, a carrier gas, e.g. nitrogen, including a cleaning enhancement substance, e.g. traces of polar organic compounds, is introduced (450) and mixes with the water which creates a gradient that aids in removing the water.

USE/ADVANTAGE - For mfr. of medical devices, disks and heads, flat panel displays, **microelectronic** masks. Removes amt. of particles on **wafer** surface and also cleans **wafer** in-situ.
Dwg.5/12

L31 ANSWER 12 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1995-055670 [08] WPIX
DNN N1995-043859
TI Semiconductor device, e.g. transistor with **die** bonding structure between **lead frames** - has bonding pads over transistor **chips** and **connects** them to lead terminals with bonding wire through shortest distance.
DC U11
IN HIGUCHI, Y; KUMANO, H
PA (ROHL) ROHM CO LTD
CYC 2
PI JP 06333976 A 19941202 (199508)* 5p
US 5666009 A 19970909 (199742) 10p
ADT JP 06333976 A JP 1993-122285 19930525; US 5666009 A Cont of US 1994-242637 19940513, US 1996-661144 19960610
PRAI JP 1993-122285 19930525
AB JP 06333976 A UPAB: 19950301
The semiconductor device includes a transistor **chip** (1) on a **mounting** unit (3) of a **lead frame** (2). The emitter side bonding pad (4) and base side bonding pad (5) are formed over the transistor **chip**. Islands (6a,7a) formed on the **lead frame** are **connected** to the bonding pads through the aluminium bonding wire (8) in a straight line. The collector electrode formed in the bottom surface of the transistor **chip** is **connected** electrically to the **mounting** unit. The **chip**, **mounting** unit, lead wires and islands are then sealed. The three lead terminals (6,7,3a) are used as the emitter, base and collector terminal respectively.

ADVANTAGE - Reduces wire length required for bonding. Increases rate of production per unit time. Increases emitter **active region**. Minimises size and cost of product.
Dwg.1/8

L31 ANSWER 13 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1994-231560 [28] WPIX

DNN N1994-183043 DNC C1994-105688
TI **Lead frame** - process for producing it, and semiconductor package.
DC A85 L03 U11
PA (SUMS) SUMITOMO SPECIAL METALS CO LTD
CYC 1
PI JP 06169051 A 19940614 (199428)* 10p
ADT JP 06169051 A JP 1992-341622 19921127
PRAI JP 1992-341622 19921127
AB JP 06169051 A UPAB: 19940831
Lead frame is fabricated by bond-lamination of (a) earth layer having leads projecting from its periphery and (b) **lead frame** layer having, in the space inside the inner tips of radially arranged **leads**, a square **frame**-shaped power source layer **connected** with power source leads and separated from other leads with (c) intermediary heat-resistant insulating resin layer covering the power source layer and a part of each lead. Leads of the earth layer are **connected** with earthing leads of the **lead frame** layer. On the **lead frame** layer (excepting central part of the power source layer), signal circuit layer composed of thin film of Al or Cu and intermediary insulator layer composed of thin film of heat resistant resin or ceramics is formed as the inner leads.

A thin film layer for wire bonding is formed at least on the semiconductor-ship-earthing surface of the earth layer material, followed by coating the prescribed area with heat resistant insulating resin (pref. heat resistant epoxy resin). A thin film layer for wire bonding is formed on the square power **source area** and other necessary parts of the **lead frame** material, followed by forming thin layer of heat resistant resin or ceramics on the prescribed parts (excepting central parts of the square power **source area**). The earth layer material and the **lead frame** material are bonded together by means of the insulating resin layer between them. Inner leads of Al (or Cu) thin film are formed on the thin layer of heat resistant resin (or ceramics) followed by **connecting** leads of the earth layer material with those of the **lead frame** material.

USE/ADVANTAGE - The **lead frame** is applicable to multiple-pin type QFP (Quad Flat Package). It permits highly precise integration of **microcircuits**.
Dwg.1/3

L31 ANSWER 14 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1994-144317 [17] WPIX
DNN N1994-113675
TI Producing semiconductor device with leads formed directly on **chip** - avoiding use of **lead-frame** by assigning area to conductors to which lead wires are bonded and used for **mounting** semiconductor device.
DC U11
IN KEE, D R
PA (TEXI) TEXAS INSTR INC
CYC 1
PI US 5308797 A 19940503 (199417)* 5p
ADT US 5308797 A US 1992-980824 19921124
PRAI US 1992-980824 19921124
AB US 5308797 A UPAB: 19940613
The semiconductor device (10) has an **active area** (12), which is the actual device, and a periphery area (11) of the material of

the semiconductor device, e.g. silicon. Conductors (14) can be deposited on the **wafer** and **connected** to the contacts (13) on the active surface.

Interconnections can be formed on the surface of an **integrated circuit** to **connect** various components. The peripheral area is either a non-conducting area or has a layer of material to prevent conduction between the conductors and the **active area**. The surface of the device is encapsulated to leave only the conductors exposed. The lead wires (15) can be ultrasonically welded to the conductors, shaped and then cut to length.

Dwg.2,3/3

L31 ANSWER 15 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1993-251034 [32] WPIX
CR 1998-263559 [24]
DNN N1993-193385
TI Lead-on-**chip** semiconductor device - has multiple leads interspersed with multiple bond pads located at **chip** periphery, with central portions of leads **connected** by wire to bond pads and inner portions extending over active surface.
DC U11 U14
IN AFSHAR, D D; BIGLER, C G; CASTO, J J; MCSHANE, M B
PA (MOTI) MOTOROLA INC
CYC 8
PI EP 554742 A2 19930811 (199332)* EN 9p
R: DE FR GB IT
JP 05275606 A 19931022 (199347)
US 5381036 A 19950110 (199508) 8p
EP 554742 A3 19930908 (199509)
US 5455200 A 19951003 (199545) 8p
SG 46298 A1 19980220 (199821)
EP 554742 B1 19980930 (199843) EN
R: DE FR GB IT
DE 69321266 E 19981105 (199850)
JP 3161128 B2 20010425 (200126) 7p
KR 276781 B 20010115 (200206)
ADT EP 554742 A2 EP 1993-101062 19930125; JP 05275606 A JP 1993-29684 19930127; US 5381036 A Cont of US 1992-829870 19920203, US 1993-107412 19930816; EP 554742 A3 EP 1993-101062 19930125; US 5455200 A Div ex US 1992-829870 19920203, US 1993-97505 19930727; SG 46298 A1 SG 1996-2328 19930125; EP 554742 B1 EP 1993-101062 19930125, Related to EP 1998-102613 19930125; DE 69321266 E DE 1993-621266 19930125, EP 1993-101062 19930125; JP 3161128 B2 JP 1993-29684 19930127; KR 276781 B KR 1993-791 19930121
FDT EP 554742 B1 Related to EP 843356; DE 69321266 E Based on EP 554742; JP 3161128 B2 Previous Publ. JP 05275606; KR 276781 B Previous Publ. KR 93018704
PRAI US 1992-829870 19920203; US 1993-107412 19930816; US 1993-97505 19930727
AB EP 554742 A UPAB: 20020128
The semiconductor device has multiple bond pads formed along the edge of the **chip** active surface. Multiple leads (24) have central portions (36) electrically **coupled** to the **chip** peripheral bond pads (14) by conductive wires (30). Inner portion (38) of the leads extends towards the centre line A-A of the active surface of the **chip** (12). Outer portion (42) of the leads extends away from the **chip**.

Pref. protrusions (50) are provided on leads (16) adjacent **chip** corners for alignment. Pref. a **lead frame** is used with a tie bar (22) overlying the **active area**

of the **chip** surface. The tie bar is electrically **coupled** to at least one bond pad (28) to serve as a voltage distribution bar.

USE/ADVANTAGE - Esp. for SRAM and DRAM, accommodating variety of **chip** designs. Good heat dissipation. Good adhesion between **lead frame** and **chip**.

Dwg.1/3

L31 ANSWER 16 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1992-365733 [44] WPIX
DNN N1992-278771 DNC C1992-162376
TI Min. wire sweep in plastic **IC** package - bond wire angle gives max. clearance over bus-bars in 16, mega bit LOC packages.
DC A32 A85 L03 U11
IN LIAN, S C; LIM, T B
PA (TEXI) TEXAS INSTR INC
CYC 1
PI US 5155578 A 19921013 (199244)* 5p
ADT US 5155578 A US 1991-691764 19910426
PRAI US 1991-691764 19910426
AB US 5155578 A UPAB: 19931006

A semiconductor device with min. bond wire distortion during encapsulation comprises a circuit **chip** having bond wires extending over an **active region**. The bond pads are along a linear path at the centre of the **chip** and positioned w.r.t. the corresponding **lead frame** fingers such that wires **connecting** the two span the active portion at 5-15 degrees to the perpendicular to the path along which the bonding pads are located. The bond wire lengths are such as to give a clearance over the **chip** of at least twice the wire dia.

Pref. the bond wires are of Au and Be; pref. the device is resin-encapsulated.

USE/ADVANTAGE - A semiconductor device with min. wire sweep (claimed) is provided which is useful for high density devices such as 16 megabit memory devices using LOC packaging technology. The wire angle gives min. sweep and max. wire clearance over the buss bars, and the staggered gating does not significantly alter the plastic flow patterns in the two adjoining cavities. The invention is also applicable to conventional packages.

1/5

L31 ANSWER 17 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1992-030107 [04] WPIX
CR 1992-030114 [04]
DNN N1993-151883 DNC C1993-087480
TI Schottky diode mfr. using diamond as a semiconductor material - invovles growing diamond on silicon substrate so that grain boundaries are excluded from the **active area**.
DC L03 U11 U12
IN HIRAKI, A; KAWARADA, H; MA, J S; YONEHARA, T
PA (CANO) CANON KK
CYC 3
PI JP 03278463 A 19911210 (199204)*
US 5219769 A 19930615 (199325)B 7p
CA 2030825 C 19951031 (199603)
ADT JP 03278463 A JP 1990-80012 19900327; US 5219769 A US 1990-617157 19901123; CA 2030825 C CA 1990-2030825 19901126
PRAI JP 1990-80012 19900327
AB JP 03278463 A UPAB: 19961007

Semiconductor element e.g. **IC** is sealed by using a hardened

epoxy resin compsn. having a moisture absorbability of upto 0.25 wt.% and a **lead-frame** bond strength at least 2.0 kgf/cm2 .

The epoxy resin compsn. pref. contains a biphenyl-type epoxy resin and dicylopentadiene-phenol polymer as a hardener, together with a hardening accelerator, a filler, a **coupling** agent, a releasing agent, and a colourant. The biphenyl-type epoxy resin is of formula (I); where is the number of repeating units, or 0 -1, and the dicyclopentadiene-phenol polymer as hardener is of formula (2), where R is H or CnH2n + 1, n is an integer and l is an integer. The epoxy resin compsn. comprises 100 pts. wt. epoxy resin, 65-120 pts.wt. hardener, 0.1-5 pts.wt. hardening accelerator, 400-1200 pts. wt. inorganic or organic filler, 1-5 pts.wt. releasing agent, and 0 -20 pts.wt. other additives.

USE/ADVANTAGE - Used as electronic parts. The device in cracking resistance of the sealing resin during soldering, moisture resistance, and heat resistance. @(8pp Dwg.No.1/2)

L31 ANSWER 18 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1991-041385 [06] WPIX
DNN N1994-214214
TI Semiconductor **integrated circuit** with reference voltage esp. in MOS memory - has substrate or well region impurity concn. in range to maintain enhancement MOS transistor mode when difference between well or substrate bias voltage and transistor source reference voltage equals built-in potential.
DC U13 U14
IN FURUYAMA, T
PA (TOKE) TOSHIBA KK
CYC 3
PI JP 02309661 A 19901225 (199106)*
US 5343087 A 19940830 (199434)B 7p
KR 9309810 B1 19931011 (199437)
ADT JP 02309661 A JP 1989-130710 19890524; US 5343087 A Cont of US 1990-520057 19900503, US 1991-713014 19910610; KR 9309810 B1 KR 1990-7523 19900524
PRAI JP 1989-130710 19890524
AB US 5343087 A UPAB: 19941013 ABEQ treated as Basic
The semiconductor **IC** includes an enhancement MOS transistor formed in a semiconductor substrate and has a substrate bias generator to supply a set bias voltage to the substrate. The substrate impurity concentration is within a range in which the enhancement MOS transistor maintains enhancement mode when the substrate potential, or difference between a voltage in the substrate and the reference voltage, equals the built-in potential phiB of the source-substrate PN junction. The MOS transistor **source region** is **coupled** to the reference voltage.

Pref. the source-**drain** separation in the MOS transistor is less than one micron, and the substrate region impurity concentration is between 1multiplied by1015cm-3 and 3multiplied by1016 cm-3. The substrate region may be a P-type well region, with an N-channel MOS transistor, having the set bias voltage lower than the reference voltage, or the transistor is a P-channel device in a N-type substrate, with bias voltage higher than the reference voltage.

USE/ADVANTAGE - E.g. DRAM; suitable for SOI. Restrained hysteresis characteristic, without increased bias generator capacitance Dwg.5/6

AB JP 02309661 A UPAB: 19941109
The **lead frame** is etched by applying an etching film, comprising a material having a faster etching rate than that of the **lead frame**, on a surface of the **lead frame** material to be etched, forming resist patterns on the

etching film, followed by etching the film and the frame material simultaneously.
USE - For etching **lead frames** having specified **leads** having rounded edge portions. @(3pp Dwg.No.1/3)@

L31 ANSWER 19 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1990-068819 [10] WPIX
DNN N1990-052707
TI Assembly packing method for sensor element - has **mounting** sensor **chips** on tape carrier, while terminal of **chips** are **connected** to corresponding electrode patterns by through holes.
DC U11 U12
IN KUMADA, A
PA (MURA) MURATA MFG CO LTD
CYC 6
PI EP 357050 A 19900307 (199010)* EN 10p
R: DE FR GB IT NL
US 4945634 A 19900807 (199034)
EP 357050 B1 19940330 (199413) EN 10p
R: DE FR GB IT NL
DE 68914214 E 19940505 (199419)
ADT EP 357050 A EP 1989-116031 19890830; US 4945634 A US 1989-400568 19890829; EP 357050 B1 EP 1989-116031 19890830; DE 68914214 E DE 1989-614214 19890830, EP 1989-116031 19890830
FDT DE 68914214 E Based on EP 357050
PRAI JP 1988-218926 19880831
AB EP 357050 A UPAB: 19930928
The method continuously provides electrode patterns which correspond to the respective terminals of sensor **chips**. patterns are located on a single side of a tape carrier composed of an insulating material. The sensor **chip** is bounded to the tape carrier. Terminals of each of the sensors are **connected** to the corresponding electrode patterns on the tape crier. The portions of the tape carrier are separated from the **mounted** sensor **chip** and location on the sensor base. A number of small through holes are formed in the tape carrier in correspondence with the respective terminals of the sensor **chips**. The sensor **chips** are fixed on the opposite side of the tape carrier relative to the electrode patterns.
ADVANTAGE - Eliminated defective mechanical strength at **connection** portion of **lead frame** which is apt to break.
1A/6

L31 ANSWER 20 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1989-257578 [36] WPIX
DNN N1989-196461
TI Hermetically sealed **integrated circuit chip** package - has metallisation which extends on one **wafer** from **connect** pads on **active** circuit **area** to extended I-O pad areas exterior of cap.
DC U11 U14
IN SAHAKIAN, V K
PA (LSIL-N) LSI LOGIC CORP
CYC 7
PI EP 331245 A 19890906 (198936)* EN 7p
R: DE ES FR GB IT
JP 01315165 A 19891220 (199006)
US 4907065 A 19900306 (199016)
EP 331245 B1 19950118 (199507) EN 10p

R: DE ES FR GB IT
DE 68920603 E 19950302 (199514)
ES 2069572 T3 19950516 (199526)
ADT EP 331245 A EP 1989-200445 19890222; US 4907065 A US 1988-162716 19880301; EP 331245 B1 EP 1989-200445 19890222; DE 68920603 E DE 1989-620603 19890222, EP 1989-200445 19890222; ES 2069572 T3 EP 1989-200445 19890222
FDT DE 68920603 E Based on EP 331245; ES 2069572 T3 Based on EP 331245
PRAI US 1988-162716 19880301
AB EP 331245 A UPAB: 19930923
The **chip** assembly comprises a generally rectangular **active chip area** in a semiconductor material, the area having desired **integrated circuit** components in it and interconnect metallisation on it. An integral band area of a predetermined width of the semiconductor material peripherally surrounds the **active chip area**. A series of spaced **integrated circuit chip** input/output pad areas extends along the band area and is **connected** to the metallisation.

A discrete cap of semiconductor material extends above and spatially covers the **active chip area**, the cap including a peripheral edge portion sealingly **affixed** around an inner periphery of the integral band area, so that the **active chip area** is protected by the cap and the input/output pad areas are exposed outside the resultant capped **active chip area**.

ADVANTAGE - Avoids plastic encapsulation or use of ceramic housing.
2/8

L31 ANSWER 21 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1973-16200U [12] WPIX
TI **Connection** of leads to a semiconductor substrate - using a single substrate **lead frame**.
DC L03 U12
PA (INTT) ITT IND INC
CYC 1
PI FR 2138325 A (197312)*
PRAI FR 1971-18623 19710524
AB FR 2138325 A UPAB: 19930831
Method of making a lead array for a semiconductor device in which **connection** pads are formed on a semiconductor substrate at its periphery and a number of flexible metal leads are **connected** to the pads extending inwards towards the **active regions** and the part of the conductor covering the pad is **joined** it. One or more wires may then be **connected** to each pad. The method provides a lead array on the same substrate as the **integrated circuit**.

L31 ANSWER 22 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 1999-289044 JAPIO
TI SEMICONDUCTOR DEVICE FOR SWITCHING POWER SOURCE CONTROL
IN SAITO TAKASHI
PA FUJI ELECTRIC CO LTD
PI JP 11289044 A 19991019 Heisei
AI JP1998-091295 (JP10091295 Heisei) 19980403
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 99
AB PROBLEM TO BE SOLVED: To improve resistance to static electricity and resistance to surge.
SOLUTION: In this semiconductor device, a **lead frame** 12 is constituted of a **chip mounting** part 18 and a

terminal part 19, and a semiconductor **chip** 1 in which an MOSFET 2 being a vertical type high withstand switching transistor, a JFET 5 being a starting power supply element, and an **IC** 7 for control are integrated are **mounted** on a **chip mounting** part 18. A **drain** pad 3 of the MOSFET2 and a **drain** pad 6 of the JFET 5 are **connected** with a **drain** terminal 13 of the **lead frame** by using bonding wires 9. The **drain** pad 3 of the MOSFET 2 and the **drain** pad 6 of the JFET 5 are **connected** with the **drain** terminal 13 by using the bonding wires 9, thereby improving resistance to surge and resistance to static electricity.

L31 ANSWER 23 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 1999-040704 JAPIO
TI SEMICONDUCTOR DEVICE
IN HOZOJI HIROYUKI; TSUNODA SHIGEHARU; SAEKI JUNICHI
PA HITACHI LTD, JP (CO 000510)
PI JP 11040704 A 19990212 Heisei
AI JP1997-189455 (JP09189455 Heisei) 19970715
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 99, No. 2
AB PURPOSE: TO BE SOLVED:To **drain** the expanded water content, without breaking a resin layer, to ensure a reliability of the semiconductor device by using a porous adhesive sheet for adhering semiconductor elements to a **die** pad; part of the sheet is exposed from a resin seal of the device.
CONSTITUTION: miconductor element 1 is adhered to a **die** pad of a **lead frame** through a porous adhesive film 3 as adhesives, and **connected** to inner leads of the **lead frame** through Au wires 4, etc., and sealed with a resin 5. The film 3 is exposed from the resin seal within an extent not influencing on the wire bonding. If absorbed water content is expanded at **mounting** of a semiconductor device, the water content is drained through fibers or holes **connected** to outside of the film 3, thereby hardly causing the peel of a resin layer or substrate or package cracks.

L31 ANSWER 24 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 1996-316737 JAPIO
TI MIXER CIRCUIT
IN TANAKA SATOSHI; IMAKADO YOSHITAKA
PA HITACHI LTD, JP (CO 000510)
PI JP 08316737 A 19961129 Heisei
AI JP1995-122149 (JP07122149 Heisei) 19950522
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 96, No. 11
AB PURPOSE: To obtain the mixer circuit with excellent linearity and less spurious radiation by **connecting** a capacitor to an **integrated circuit** between an IF terminal of an integrated mixer circuit and a ground terminal.
CONSTITUTION: A circuit part surrounded by a thick line is an **integrated circuit** and a caption Lp indicates a parasitic inductor produced at **mounting**. A capacitor C2 is **connected** between a ground terminal and a **drain** output terminal on the **integrated circuit**. Thus, the impedance of a **drain** at a high frequency is reduced. The impedance of the ground terminal on the **integrated circuit** is easily decreased by countermeasures such as the use of

a **lead frame** and use of plural bonding wires.

L31 ANSWER 25 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 1996-051179 JAPIO
TI **INTEGRATED CIRCUIT** DEVICE AND **LEAD FRAME**
IN NISHIDA MASAO; SAWAI TETSUO; UDA NAONORI; HARADA YASOO
PA SANYO ELECTRIC CO LTD, JP (CO 000188)
PI JP 08051179 A 19960220 Heisei
AI JP1994-185669 (JP06185669 Heisei) 19940808
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 96, No. 2
AB PURPOSE: To provide an **integrated circuit** device and a **lead frame** capable of scaling down the size of a **chip**.
CONSTITUTION: An input matching circuit, a source bias circuit, a **drain** bias circuit and an output matching circuit of a microwave amplifier are composed of the series **connected** inductors and capacitors or only inductors. Insulating films 3 and metallic films 4 are formed onto leads 11A, 11D, 11F, thus forming MIM structure. The MIN structure on the leads 11A, 11D, 11F and the parasitic inductance of the leads 11A, 11D, 11F constitute the series **connection**, and inductance is configured of the parasitic inductance of the leads 11B, 11E.

L31 ANSWER 26 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 1995-038046 JAPIO
TI SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE
IN YANO HIROSHI; MASUDA MASACHIKA; HAYAKAWA TAKESHI
PA HITACHI LTD, JP (CO 000510)
PI JP 07038046 A 19950207 Heisei
AI JP1993-178777 (JP05178777 Heisei) 19930720
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 95, No. 2
AB PURPOSE: To obtain a semiconductor **integrated circuit** device making it possible to prepare a normally/reversely bent article of a lead for an **active area** of a semiconductor **chip** by enabling obverse and reverse assemblies of the same **chip** by using the same usual manufacturing equipment.
CONSTITUTION: A package-shaped semiconductor **integrated circuit** device being asymmetric vertically, such as SOJ, which has a structure wherein a semiconductor **chip** 2 is **mounted** reversibly on the upper side of a **lead frame** 1 with a pellet-bonding material 3 interposed, an electrode of this semiconductor **chip** 2 and a lead of the **lead frame** 1 are **connected** by a wire 4 by bonding and further mold-sealed with resin 5 and then lead formation is conducted. A tab of the **lead frame** 1 is provided with a through hole 10, and in the case when the semiconductor **chip** 2 is **mounted** reversely in relation to the tab 6, the electrode of the semiconductor **chip** 2 and an inner lead 8 are **connected** by the wire through this through hole 10 so as to be assembled.

L31 ANSWER 27 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 1993-312847 JAPIO
TI SEMICONDUCTOR DEVICE FOR ELECTRIC CURRENT DETECTION
IN KITAMURA KAZUNARI; KAWAKAMI TAKAYOSHI
PA MITSUBISHI ELECTRIC CORP, JP (CO 000601)
PI JP 05312847 A 19931126 Heisei

AI JP1992-115942 (JP04115942 Heisei) 19920508
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 1701, Vol. 18, No. 125, P. 146 (19940228)
AB PURPOSE: To provide a highly sensitive semiconductor device for electric current detection which does not lose detection precision even if the resistance of the soldered **connection** part of a **chip** resistor.
CONSTITUTION: A control **IC** 2 and electrode parts 3a, 3b of a **chip** resistor 3 are **connected** each other by wire-bonding and circuit bonding of the **chip** resistor 3 and the control **IC** 2 is carried out by both soldering and wire-bonding. The effect of the **drift** amount of the contact resistance of the soldering part of the **chip** resistor 3 and a **lead frame** is lessened.

L31 ANSWER 28 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 1990-211659 JAPIO
TI SEMICONDUCTOR DEVICE
IN SATO KENGO; YAMADA HIROSHI; SAITO MASAYUKI
PA TOSHIBA CORP, JP (CO 000307)
PI JP 02211659 A 19900822 Heisei
AI JP1989-31085 (JP01031085 Heisei) 19890213
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 999, Vol. 14, No. 511, P. 21 (19901108)
AB PURPOSE: To lengthen an inner lead section, and to increase the strength of drawing by forming the inner-lead bonding section of a **lead frame** to the upper section of a bonding pad on the **active region** of a semiconductor element.
CONSTITUTION: A bonding pad 3 is shaped onto a protective insulating film on an **active region** 1a as the circuit region of a semiconductor element 1. The inner lead sections 4 of a **lead frame** 6 are arranged so as to be extended to the upper section of the semiconductor element 1. The bonding pad 3 and the inner lead sections 4 are **connected** by metallic small-gage wires 5, and the whole is sealed with an epoxy resin. According to the constitution, the inner lead sections sealed can be lengthened, thus increasing the strength of drawing of an **IC** socket, etc.

L31 ANSWER 29 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 1989-256188 JAPIO
TI SEMICONDUCTOR LASER DEVICE
IN WADA MASARU; ITO KUNIO
PA MATSUSHITA ELECTRIC IND CO LTD, JP (CO 000582)
PI JP 01256188 A 19891012 Heisei
AI JP1988-84715 (JP63084715 Heisei) 19880406
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 871, Vol. 14, No. 12, P. 40 (19890111)
AB PURPOSE: To realize cost reduction by fixing an Si submount bonded with a laser **chip** on a metal **lead frame** and by sealing it with a transparent molding resin.
CONSTITUTION: An Si submount 4 which is provided with a photodiode 2 and a laser **chip** 3 is fixed to one tip section of an external lead 1, and the remaining external leads are **connected** to the electrode of the photodiode 2 and the laser **chip** 3, respectively with a metal fine line. An assembly structure made in this way is sealed with transparent resin 5. Since the transparent resin 5 is prevented from entering a section of a recessed area 16 formed near an **active region** due to a surface tension thereof, the interior of the area 16 is hollow. Because the same material and process as an ordinary resin

sealed semiconductor device can be used for this manufacture, cost reduction can be realized.

L31 ANSWER 30 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 1988-221634 JAPIO
TI FIXING METHOD FOR SEMICONDUCTOR PELLET
IN SEKIDA KOICHI
PA NIPPON MINING CO LTD, JP (CO 330259)
PI JP 63221634 A 19880914 Showa
AI JP1987-55003 (JP62055003 Showa) 19870310
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 703, Vol. 13, No. 16, P. 42 (19890113)
AB PURPOSE: To improve adhesion strength, electric conductivity heat conductivity, and heat-resisting performance and to enable automation in bonding, by forming a metallic thin film on a rear of a semiconductor substrate and next covering the main surface with a protective film and forming a plating layer of a gold group alloy and cutting this substrate into pellets and welding their pellets on a supporting board. CONSTITUTION: A metallic thin film 2 is formed to serve as a base of alloy plating on a rear of a **wafer** 1 with an element **active region** formed on a main surface thereof. This metallic thin film 2 is made to be a three-layer metallic film like Ti-Pt-Au or a two layer metallic film like Cr-Au. In succession, a main surface of the **wafer** 1 is coated with a protective film 3 made of a photoresist or the like and the **wafer** 1 is soaked into an alloy plating bath to perform electrolytic plating, so that a gold group eutectic crystal alloy plating layer 4 is formed on a surface of the metallic thin film 2 which is formed on the rear of the **wafer** 1. The protective film 3 on the main surface of the **wafer** 1 is removed and the **wafer** 1 is cut into individual pellets 5. Thereafter, the respective pellets 5 are **mounted** on a supporting board 6 such as a **lead frame** or a ceramic substrate and heated. Thus, the eutectic crystal alloy plating layer 4 is fused and the pellets 5 are welded on the supporting board 6, so that **uniform** and solid adhesion is obtained.

L31 ANSWER 31 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 1988-107156 JAPIO
TI RESIN PACKAGED TYPE SEMICONDUCTOR DEVICE
IN TSUBOSAKI KUNIHIRO; SUZUKI KAZUNARI; ICHITANI MASAHIRO
PA HITACHI LTD, JP (CO 000510)
HITACHI MICRO COMPUT ENG LTD, JP (CO 470864)
PI JP 63107156 A 19880512 Showa
AI JP1986-251710 (JP61251710 Showa) 19861024
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 659, Vol. 12, No. 348, P. 165 (19880919)
AB PURPOSE: To prevent breakdown of bonding wires at the time of temperature cycles and to prevent cracks in molding resin, by providing a **chip** coating film on a semiconductor **chip** on the side of an **active region**, and specifying the Young's modulus (modulus of longitudinal elasticity) of the **chip** coating film. CONSTITUTION: A semiconductor **chip** 4 is **mounted** on a semiconductor-**chip attaching** substrate 2. The semiconductor **chip** 4 and a **lead frame** 1 are electrically **connected** with bonding wires 5. A **chip** coating film 6 is provided on the semiconductor **chip** 4 on the side of an **active region**. Thereafter the device is packaged with a molding resin 7. The Young's modulus of the **chip** coating film 6 is made to be 1 kg f/mm2-100 kg f/mm2. Adhesive property

with the molding resin 7 is imparted to the **chip** coating film 6. Thus the thermal strain and the thermal deformation of the molding resin (resin packaging material) 7 at the time of temperature cycle 5 can be reduced. Therefore, occurrence of breakdown of the bonding wires 5 and cracks in the resin and damage the semiconductor **chip** 4 can be prevented.

L31 ANSWER 32 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 1987-066133 JAPIO
TI TEMPERATURE SENSOR
IN KATO ATSUSHI; MIZOKOSHI YASUO; KISHIMOTO MAKOTO; WADA YOSHIHIRO
PA SHARP CORP, JP (CO 000504)
PI JP 62066133 A 19870325 Showa
AI JP1985-207991 (JP60207991 Showa) 19850918
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 609, Vol. 11, No. 261, P. 14 (19870825)
AB PURPOSE: To reduce the variation of a resistance value against an external distortion or stress by **connecting** the third lead loaded with a standard resistor, to one of two leads **connected** to two electrodes of a heat sensitive element.
CONSTITUTION: A **lead frame** 3 is **connected** to two electrodes of a heat sensitive element 1, and a square type **chip** resistor 2' of 5K.OMEGA. and a square type **chip** resistor 2 of 23K.OMEGA. are **connected** so as to be orthogonal to each other, to a terminal 3b in the middle of said frame, and a **connecting** part of a terminal 3c and the terminal 3b, respectively. In points C of three parts, half etching of about 60% is performed to the **lead frame** 3, and 0.15mm of the original thickness is converted to 0.06mm. Accordingly, a resistance value **drift** caused by a fact that an external distortion or stress is applied to a lead loaded with a **chip** resistor, in a production stage, etc. is suppressed, and a resistance measuring mistake and falling of the resistor can be prevented.

L31 ANSWER 33 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 1982-107043 JAPIO
TI SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE
IN SATAKE TOMOMITSU
PA NEC CORP, JP (CO 000423)
PI JP 57107043 A 19820703 Showa
AI JP1980-184575 (JP55184575 Showa) 19801225
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 135, Vol. 6, No. 2, P. 6 (19821009)
AB PURPOSE: To increase a protective effect for a **chip** and prevent a short-circuit of **lead frame** by **attaching** and forming an insulated organism layer onto an **active region** and a dicing region of a **chip** having a projecting electrode **mounted** thereon.
CONSTITUTION: For example, a polyimide resin film 6 is **attached** to the entire surface of a **wafer** 5 having a projecting electrode 3 **mounted** thereon through a barrier metallic layer 2 and a resist mask 8 is provided on a **region** covering the **active region** and a dicing region line 4 of a **chip** 9. Subsequently, a resin layer 6 on the region of the projecting electrode 3 is removed through an etching, thereafter the resin layer 6 is divided into the **chips** 9 and a **lead frame** 10 is **connected** through a heat pressing to the projecting electrode 3. In such a way, exposure of Si to the **chip** end can be prevented by **mounting** the resin film 6 at the most

external circumference 11 of the **chip** and consequently occurrence of a short-circuit with the **lead frame** 10 can be prevented and a yield also be improved.

L31 ANSWER 34 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 1982-103336 JAPIO
TI SEMICONDUCTOR DEVICE
IN UTSUKI ATSUSHI; MATSUBARA TOSHIAKI
PA HITACHI LTD, JP (CO 000510)
HITACHI TOBU SEMICONDUCTOR LTD, JP (CO 470867)
PI JP 57103336 A 19820626 Showa
AI JP1980-178849 (JP55178849 Showa) 19801219
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 133, Vol. 6, No. 1891, P. 115 (19820928)
AB PURPOSE: To obtain a resin molded semiconductor device having small temperature **drift** by absorbing the resin stress change to a **chip** coating material by covering a **mounted** pellet with the **chip** coating material when the pellet is **mounted** at the pellet **mounting** unit of a **lead frame** with silver paste.
CONSTITUTION: A paste 16 of semiconductor **chip** is **mounted** via silver paste on a tab 12 of the pellet **mounting** unit of a **lead frame** 10, and the electrode of the pellet 16 is electrically **connected** to the inner **lead** of the **frame** 10 via a wire 18. Thereafter, they are molded with molding resin 22, and a dome-shaped **chip** coating material 20 is covered on the periphery of the pellet 16 at this time. Thus, the stress from the resin 22 can be absorbed by the coating material 20, the stress is not applied directly to the pellet 16, and the temperature hysteresis phenomenon such as offset voltage can be remarkably reduced.